

COMPAL CONFIDENTIAL

MODEL NAME : AAPA0

PCB NO : LA-C541P

BOM P/N : 4319X031L01

GPIO MAP: Gen7 GPIO Master_0612

MIRAMAR 15"

Skylake H-type (2 chip)

REV : 1.0(A00)

2015.08.17

@, @EMC@ : Nopop Component

EMC@ : EMI/ESD/RF part

AAC@ : pop AAC config

XDP@ : Total debug Component (pop them until ST)

CONN@ : Connector Component

@AAC@ : Nopop AAC config(control by EC)

Layout Dell logo



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REV: X00
PWB: XXXXX
DATE: 1448-02

PCB 1DI LA-C541P REV0 M/B

Part Number	Description
DAA000A2010	PCB 1DI LA-C541P REV1 M/B

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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+PWR_SRC +5V_ALW +3.3V_ALW +3.3V_ALW2 +3.3V_ALW_DSW +3.3V_ALW_PCH +3.3V_RTC_LDO +1.8V_ALW +1.0V_PRIM	+3.3V_SUS +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +1.5V_RUN +0.675V_DDR_VTT +3.3V_MXM +5V_MXM +MXM_PWR_SRC	+3.3V_M (M-OFF) +3.3V_M +VCC_CORE +VCC_EDRAM +VCC_EOPIO +VCC_GTU +VCC_GT +1.0V_VCCSTG +VCC_SA
S0	ON	ON	ON	ON
S3	ON	ON	OFF	ON
S5 S4/AC	ON	OFF	OFF	ON
S5 S4/AC don't exist	OFF	OFF	OFF	OFF

SATA	DESTINATION
SATA 0	SSD 2280
SATA 1	Dock ESATA
SATA 2	NA
SATA 3	SATAe HDD
SATA 4	M.2 Slot-2(cache)
SATA 5	NA

USB PORT#	DESTINATION
1	Left Side JUSB1
2	Right Side JUSB1
3	Right Side JUSB2
4	Right Side JUSB3
5	Docking USB3.0
6	M.2 Slot-1 (BT)
7	Docking USB 2.0
8	M.2 Slot-2 (WWAN/LTE/HCA)
9	Touch Screen
10	LYNX(CV2)
11	Camera
12	NA
13	NA
14	NA

LYNX(CV2)	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	NA
Lane 2	M.2 Slot-1 (WLAN)
Lane 3	MMI(Card reader)
Lane 4	10/100/1G LOM
Lane 5~8	TBT-Alpine Ridge
Lane 9~12	M.2 Slot-3 (SSD 2280)
Lane 13~14	(Dock ESATA),NA(LANE reservsal)
Lane 15~16	SATA-Express HDD(LANE reservsal)
Lane 17~18	M.2 Slot-2 (WWAN/LTE/HCA)

Stack up

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil
			SolderMask	IT-158
			Add Plating	
1	Top	3.7	Copper foil	0.5oz
2	GND/PWR	3.7	Prepreg	1080
		3.7	Copper foil	1oz
3	Sig 1	4.1	Core	4mil
		4.1	Copper foil	1oz
4	GND/PWR	3.7	Prepreg	2116Mx2
		3.7	Copper foil	1oz
5	Sig 2	3.8	Core	4mil
		3.8	Copper foil	1oz
6	Sig 3	3.7	Prepreg	1080Hx2
		3.7	Copper foil	1oz
7	GND/PWR	4.1	Core	4mil
		4.1	Copper foil	1oz
8	Sig 4	3.7	Prepreg	2116Mx2
		3.7	Copper foil	1oz
9	GND/PWR	3.7	Core	4mil
		3.7	Copper foil	1oz
10	Bottom	3.7	Prepreg	1080
		3.7	Copper foil	0.5oz
			Add Plating	
			SolderMask	
Overall Thickness (1.45mm ± 10%)				57.09

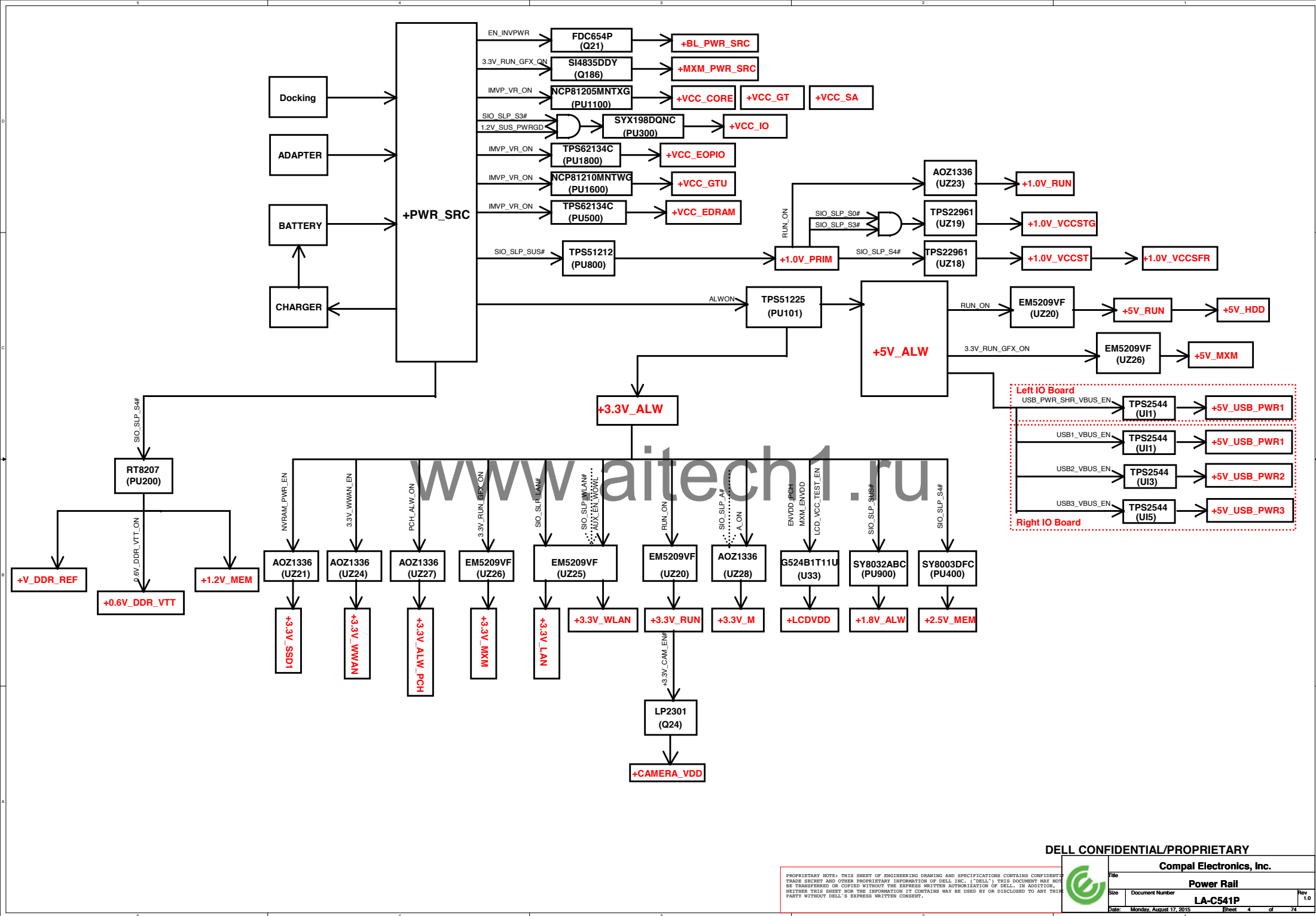
USB3.0	DESTINATION
Port 1	Left Side JUSB1
Port 2	M.2 Slot-2 (WWAN/LTE/HCA)
Port 3	Right Side JUSB1
Port 4	Right Side JUSB2
Port 5	Right Side JUSB3
Port 6	Docking

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Power Rail

LA-C541P

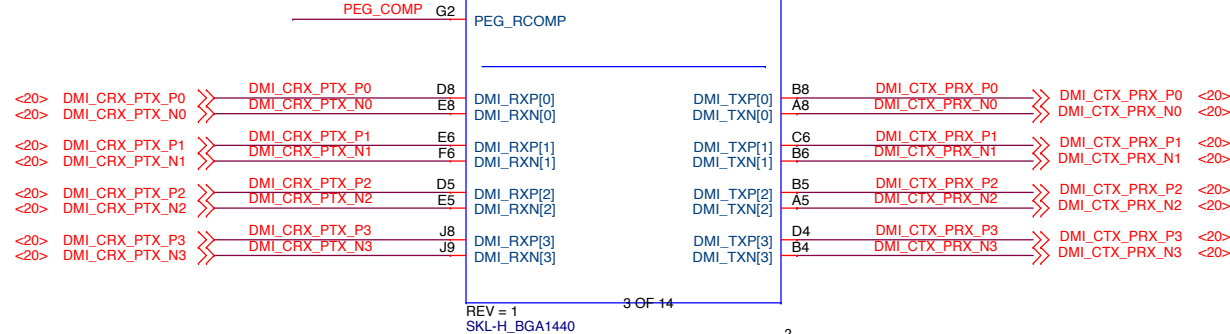
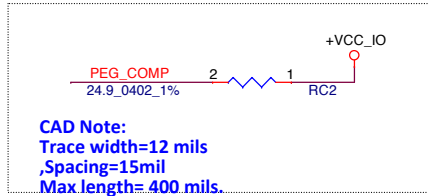
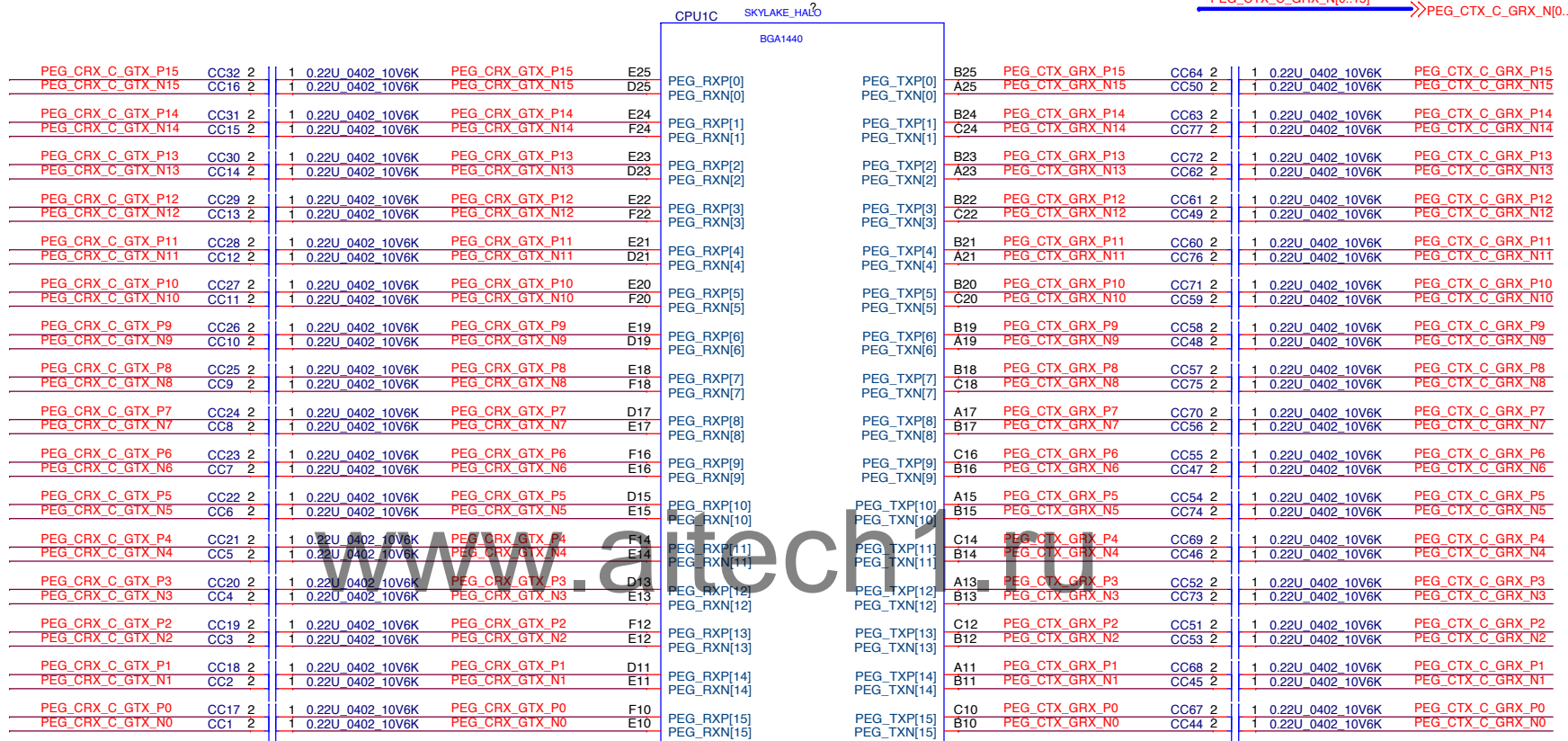
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PEG_CRX_C_GTX_N[0..15] << PEG_CRX_C_GTX_N[0..15] <18>
PEG_CTX_C_GRX_P[0..15] >> PEG_CTX_C_GRX_P[0..15] <18>
PEG_CTX_C_GRX_N[0..15] >> PEG_CTX_C_GRX_N[0..15] <18>



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SKL-H (1/8)

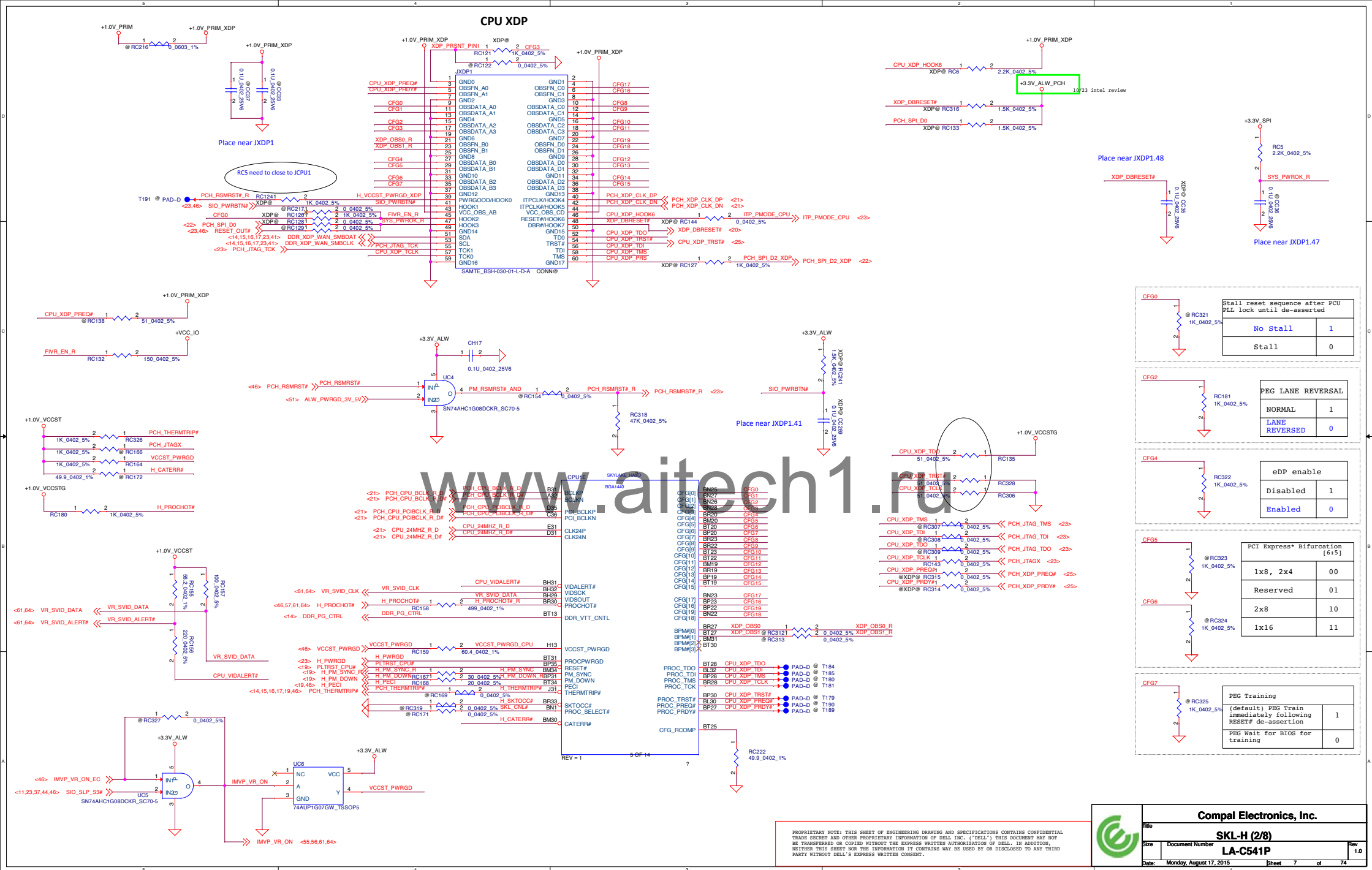
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CPU XDP



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SKL-H (2/8)

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Dock Port1

<31> CPU_DP1_P0
<31> CPU_DP1_N0
<31> CPU_DP1_P1
<31> CPU_DP1_N1
<31> CPU_DP1_P2
<31> CPU_DP1_N2
<31> CPU_DP1_P3
<31> CPU_DP1_N3

<31> CPU_DP1_AUXP
<31> CPU_DP1_AUXN

TBT

<34> CPU_DP2_P0
<34> CPU_DP2_N0
<34> CPU_DP2_P1
<34> CPU_DP2_N1
<34> CPU_DP2_P2
<34> CPU_DP2_N2
<34> CPU_DP2_P3
<34> CPU_DP2_N3

<34> CPU_DP2_AUXP
<34> CPU_DP2_AUXN

mDP/TBT

<33> CPU_DP3_P0
<33> CPU_DP3_N0
<33> CPU_DP3_P1
<33> CPU_DP3_N1
<33> CPU_DP3_P2
<33> CPU_DP3_N2
<33> CPU_DP3_P3
<33> CPU_DP3_N3

<33> CPU_DP3_AUXP
<33> CPU_DP3_AUXN

CPU_DP1_P0 K36
CPU_DP1_N0 K37
CPU_DP1_P1 J35
CPU_DP1_N1 J34
CPU_DP1_P2 H37
CPU_DP1_N2 H36
CPU_DP1_P3 J37
CPU_DP1_N3 J38

CPU_DP1_AUXP D27
CPU_DP1_AUXN E27

CPU_DP2_P0 H34
CPU_DP2_N0 H33
CPU_DP2_P1 F37
CPU_DP2_N1 G38
CPU_DP2_P2 F34
CPU_DP2_N2 F35
CPU_DP2_P3 E37
CPU_DP2_N3 E36

CPU_DP2_AUXP F26
CPU_DP2_AUXN E26

CPU_DP3_P0 C34
CPU_DP3_N0 D34
CPU_DP3_P1 B36
CPU_DP3_N1 B34
CPU_DP3_P2 F33
CPU_DP3_N2 E33
CPU_DP3_P3 C33
CPU_DP3_N3 B33

CPU_DP3_AUXP A27
CPU_DP3_AUXN B27

CPU1D SKYLAKE_HALO

BGA1440

DDI1_TXP[0]
DDI1_TXN[0]
DDI1_TXP[1]
DDI1_TXN[1]
DDI1_TXP[2]
DDI1_TXN[2]
DDI1_TXP[3]
DDI1_TXN[3]

DDI1_AUXP
DDI1_AUXN

EDP_DISP_UTIL

EDP_RCOMP

PROC_AUDIO_CLK
PROC_AUDIO_SDI
PROC_AUDIO_SDO

D29 EDP_TXP0
E29 EDP_TXN0
F28 EDP_TXP1
E28 EDP_TXN1
B29 EDP_TXN2
A29 EDP_TXP2
B28 EDP_TXN3
C28 EDP_TXP3

EDP_TXP0 <29>
EDP_TXN0 <29>
EDP_TXP1 <29>
EDP_TXN1 <29>
EDP_TXN2 <29>
EDP_TXP2 <29>
EDP_TXN3 <29>
EDP_TXP3 <29>

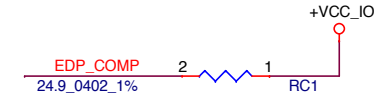
C26 EDP_AUXP
B26 EDP_AUXN

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EDP_AUXN <29>

A33 PAD~D @ T194

D37 EDP_COMP

COMPENSATION PU FOR
eDP



CAD Note:Trace width=20 mils
,Spacing=25mil,
Max length=100 mils.

G27 AUD_AZACPU_SCLK
G25 AUD_AZACPU_SDO
G29 AUD_AZACPU_SDI

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AUD_AZACPU_SDO <23>

SKL-H_BGA1440

REV=1

2

AUD_AZACPU_SDI 1
RC66

2AUD_AZACPU_SDI_R
20_0402_5%

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Rev

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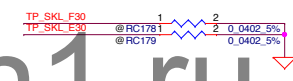
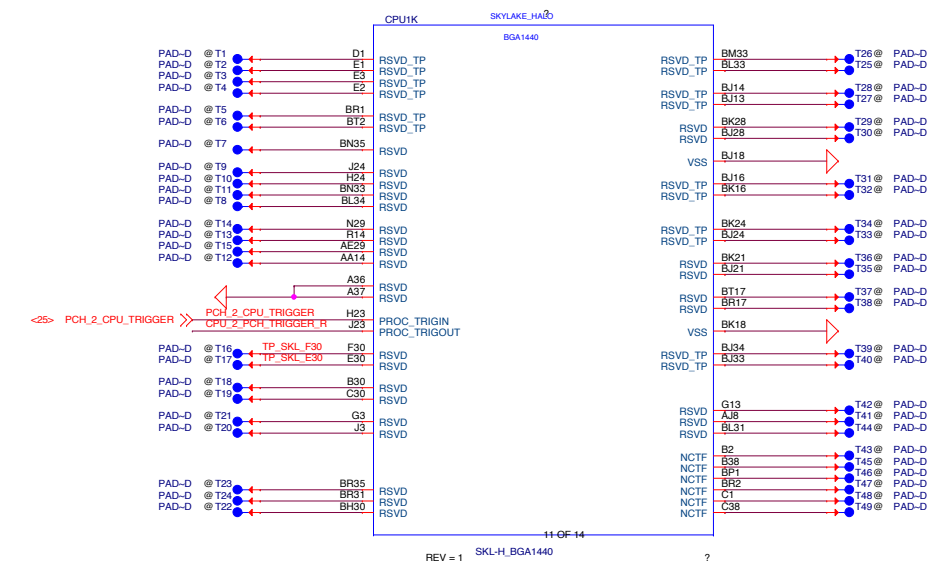
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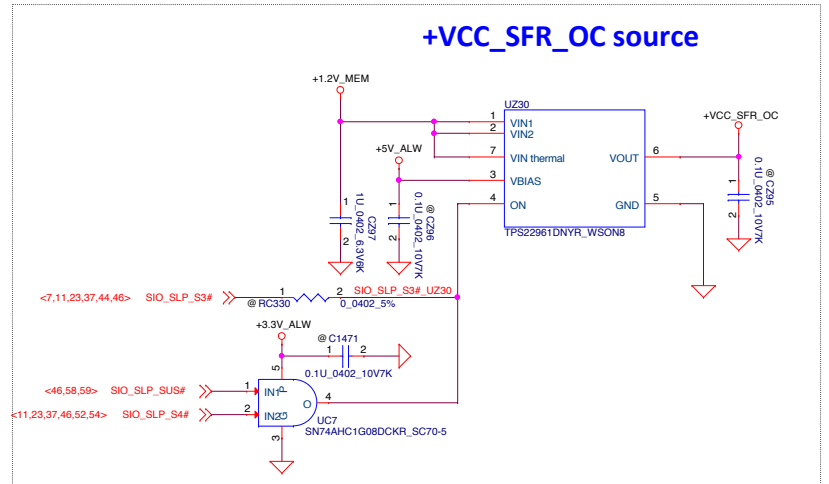
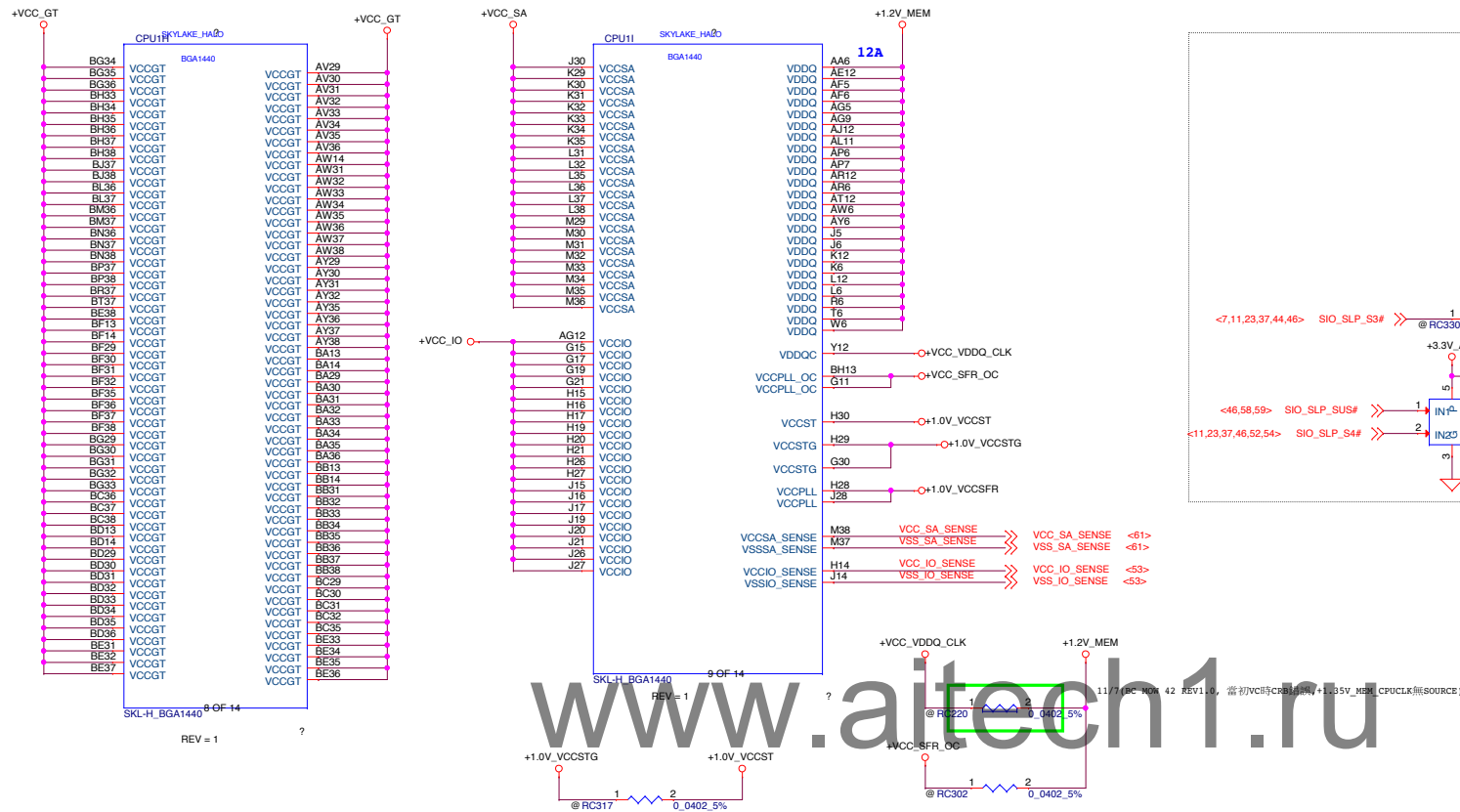
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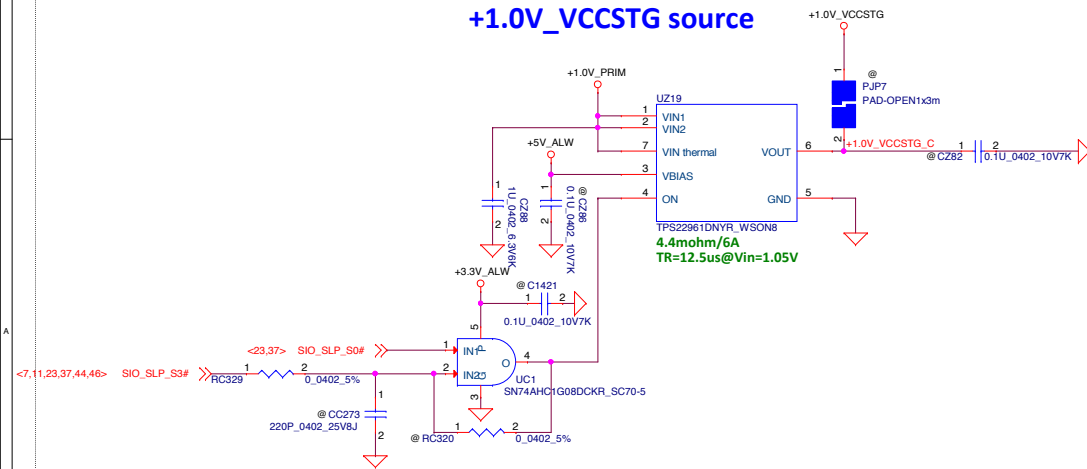
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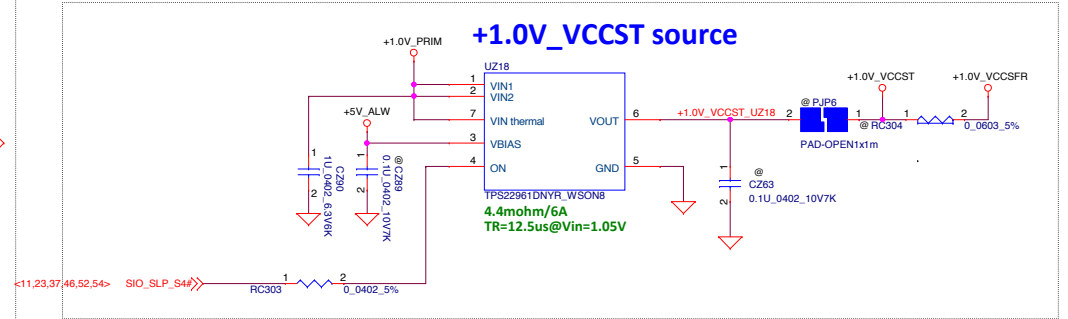




+1.0V_VCCSTG source



+1.0V_VCCST source



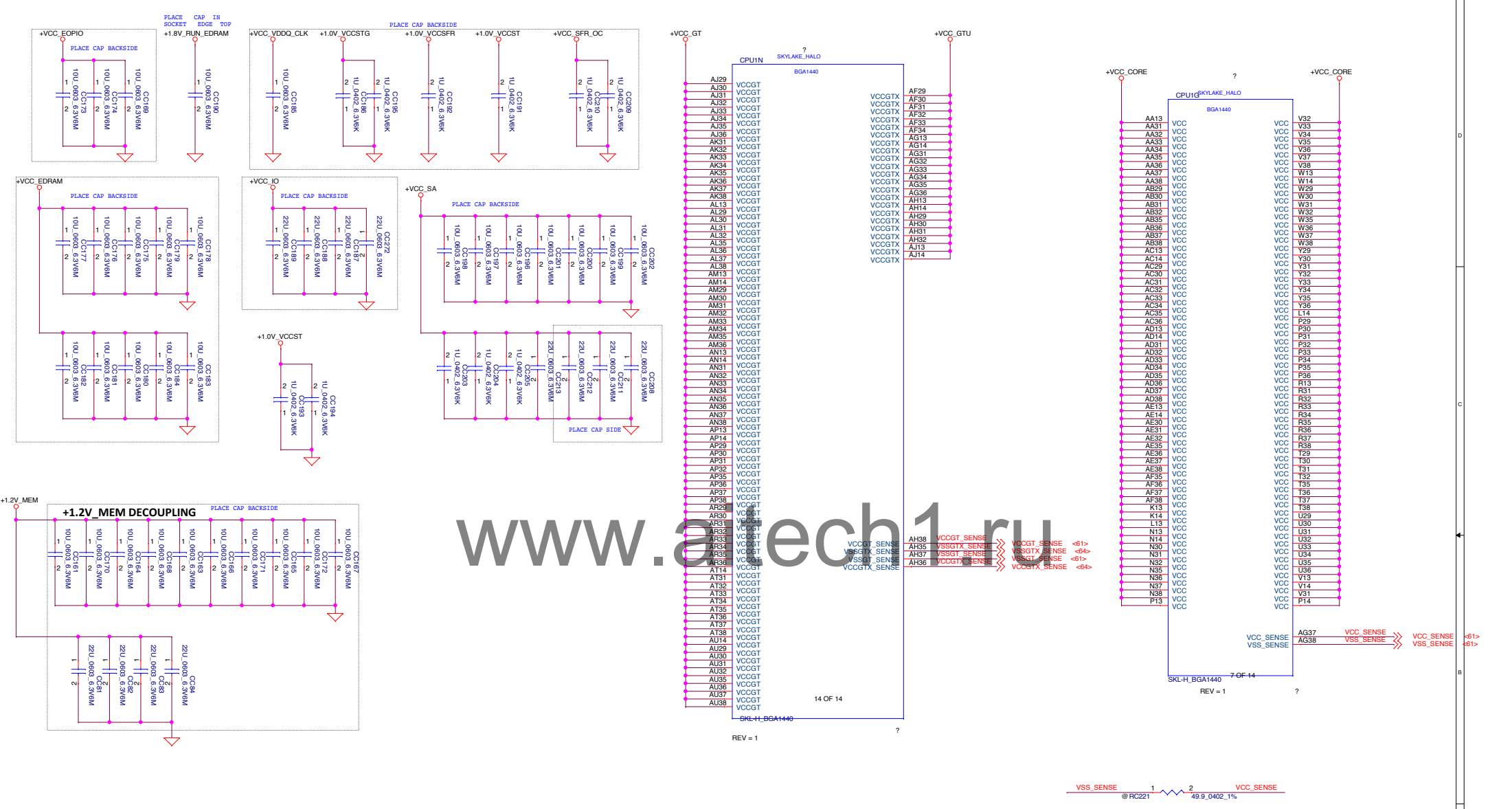
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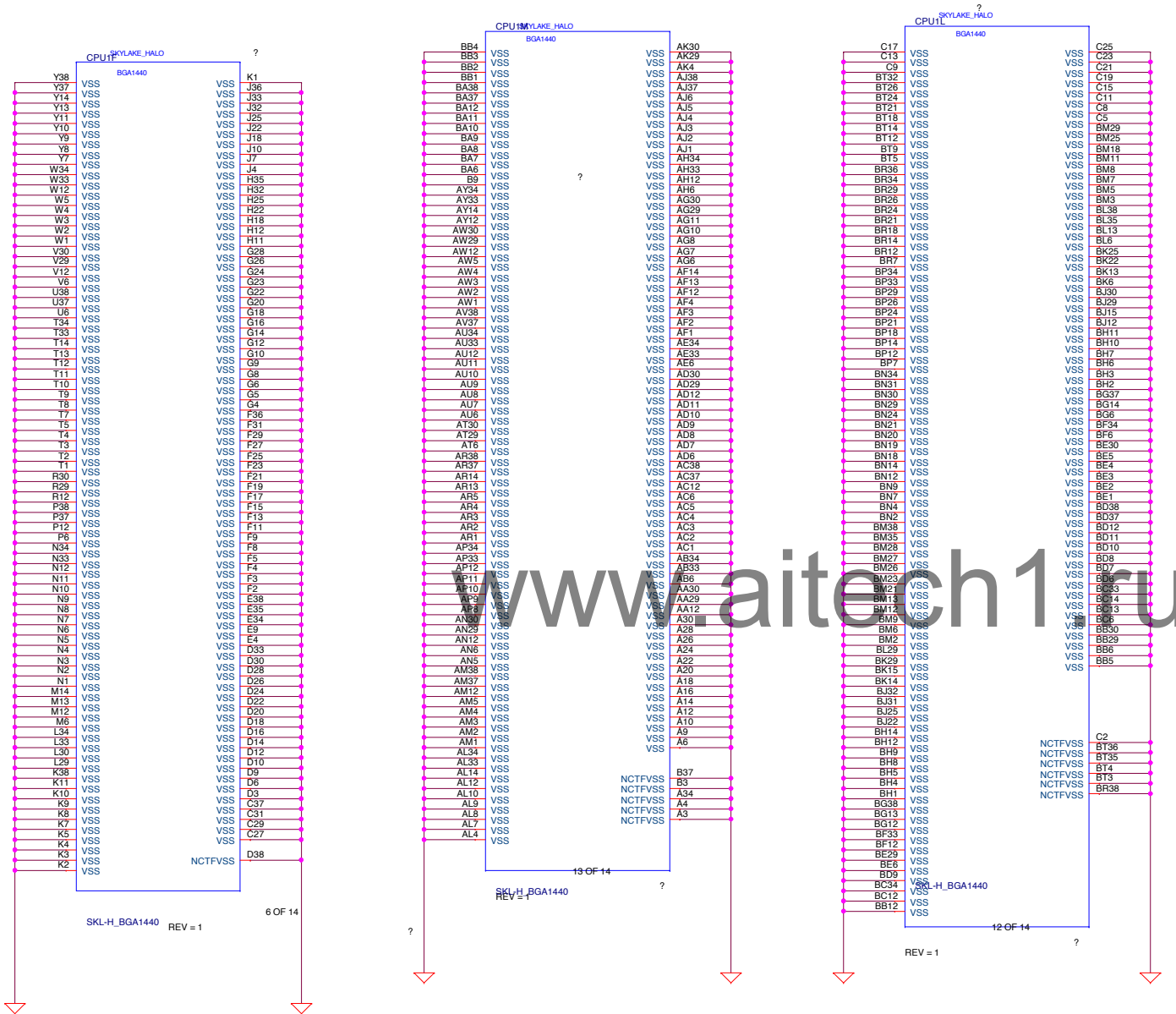


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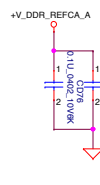
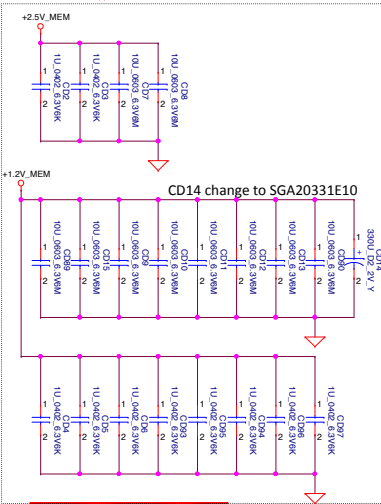
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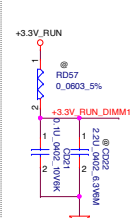
Rev 1.0

Populate RD1, De-Populate RD2 for Intel
DDR3
VREFDQ multiple methods M1
Populate RD2, De-Populate RD1 for Intel
DDR3
VREFDQ multiple methods M3



The schematic shows a 3.3V RUN power plane with a mesh of resistors (RD17, RD13, RD8, RD30, RD29, RD28) and DIMM1 memory modules connected to SA0, SA1, and SA2. The resistors are labeled with values like 0.0402_5%.

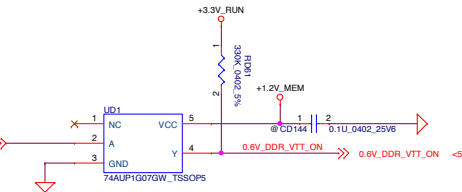
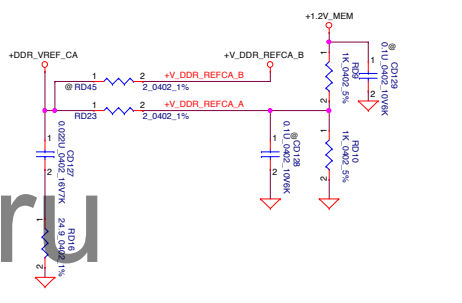
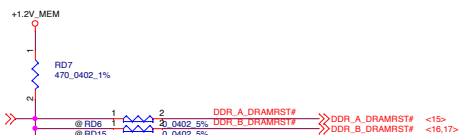
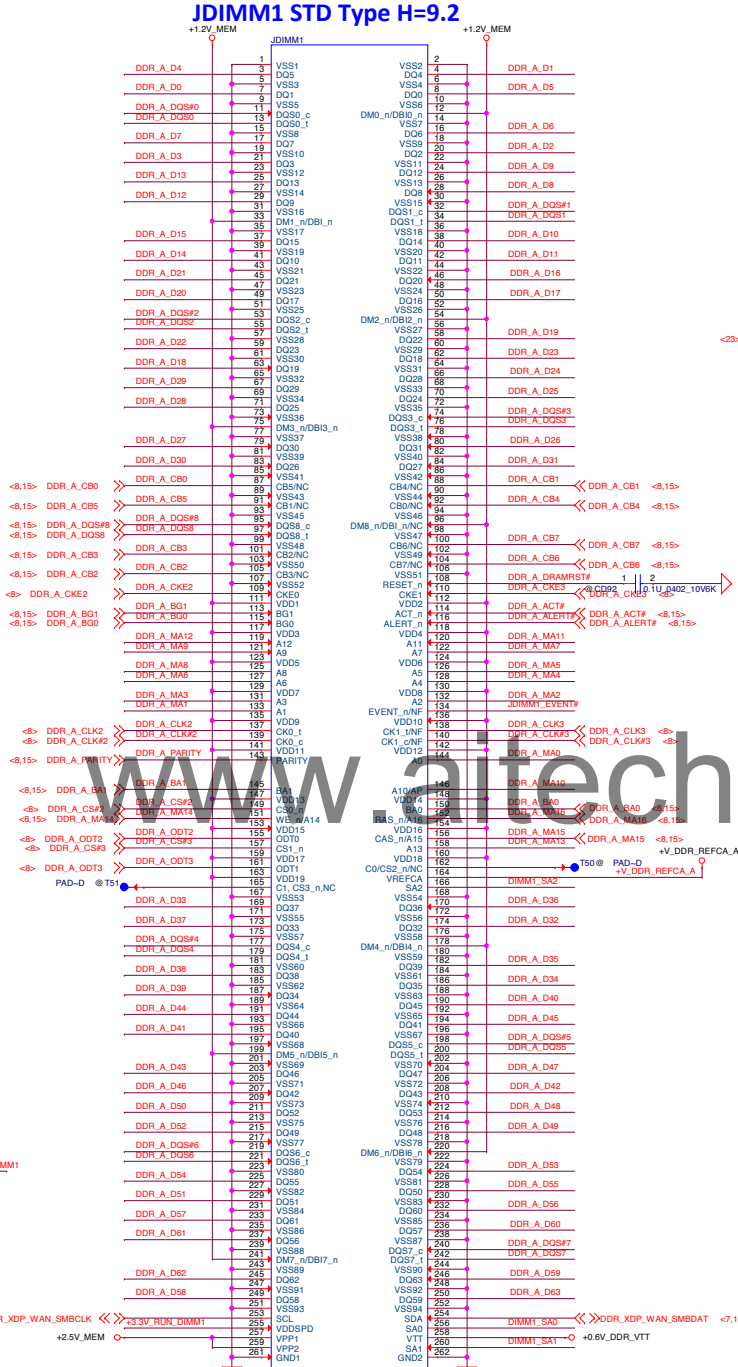
	SA0	SA1	SA2
* DIMM1	1	0	0
DIMM2	0	0	0
DIMM3	1	1	0
DIMM4	0	1	0



+2.5V MEM



CONN LIST1020



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DDR4-SODIMM SLOT1

LA-C541F

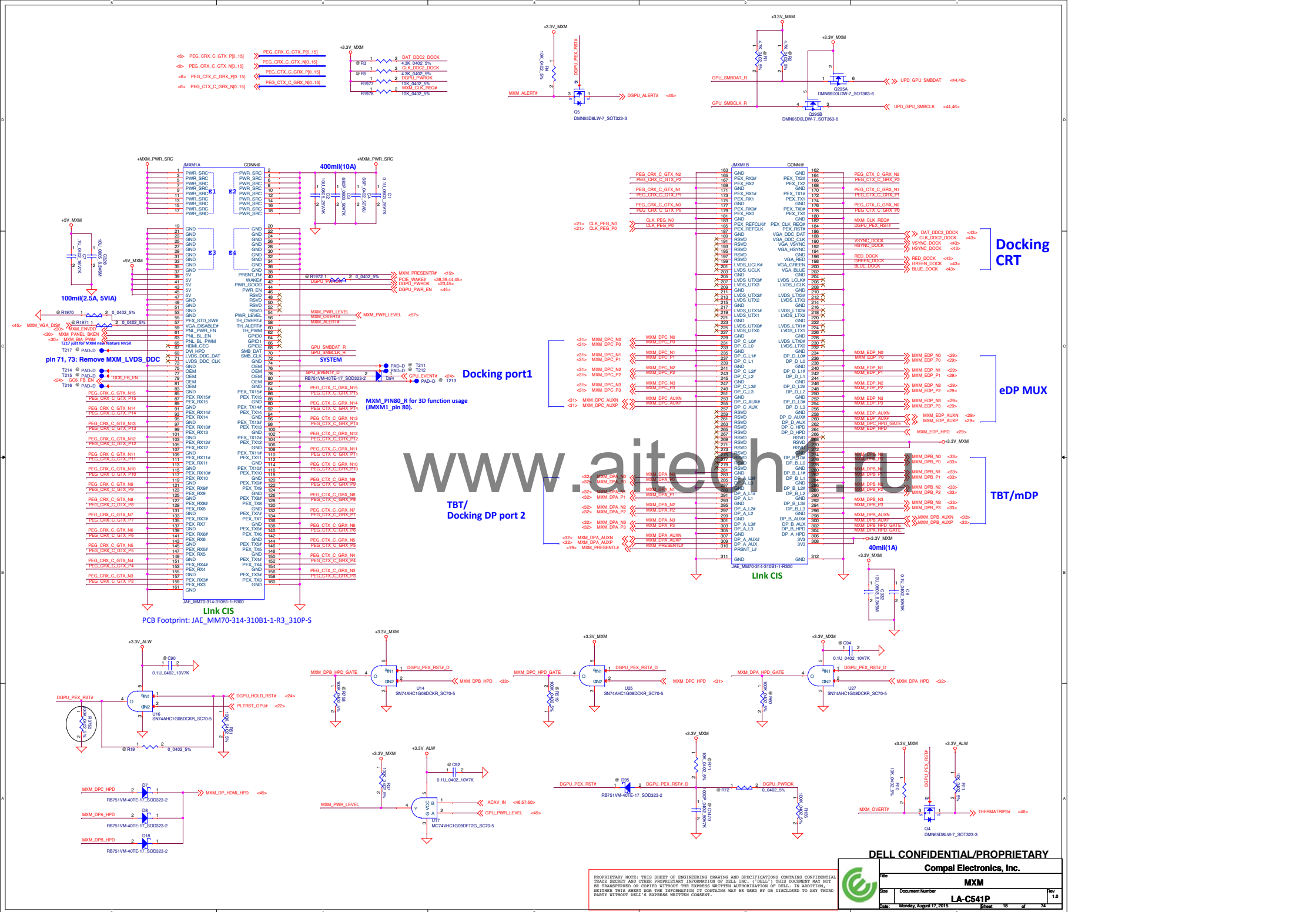
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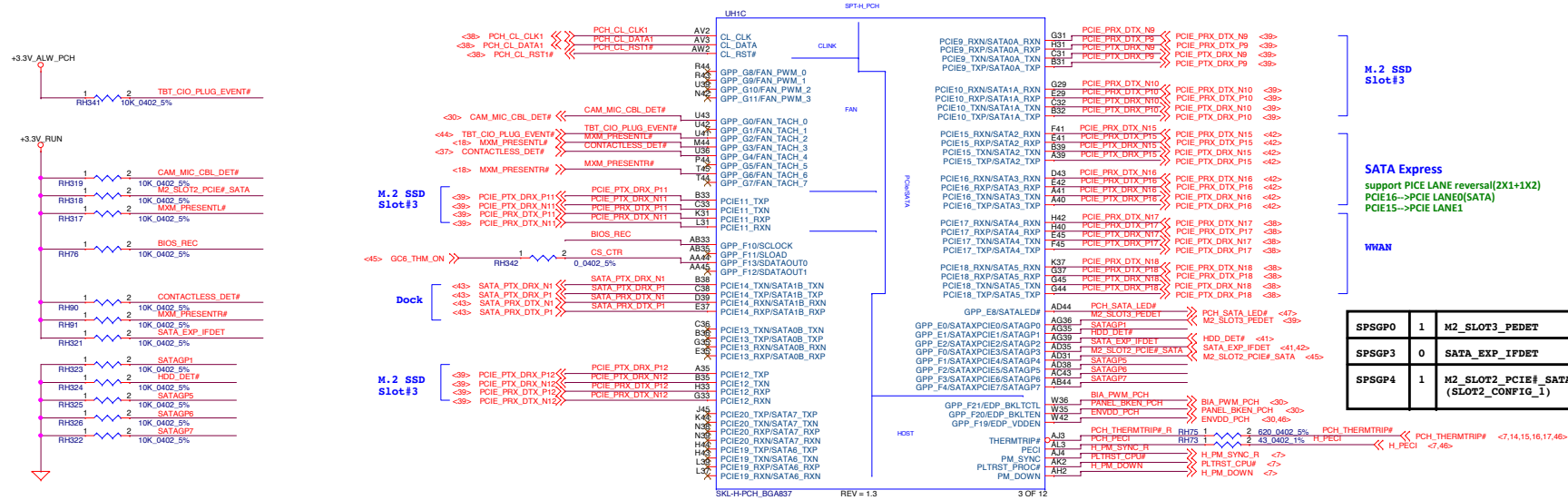
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+1.2V_MEM JDIMM3





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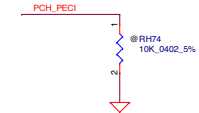
M.2 SSD Slot#3

SATA Express

support PICE LANE reversal(2X1+1X2)
PCIE16->PCIE LANE0(SATA)
PCIE15->PCIE LANE1

WLAN

SPSGP0	1	M2_SLOT3_PEDET	0=SATA 1=PCIE
SPSGP3	0	SATA_EXP_IFDET	0=SATA 1=PCIE
SPSGP4	1	M2_SLOT2_PCIE#_SATA (SLOT2_CONFIG_I)	0=SATA 1=PCIE



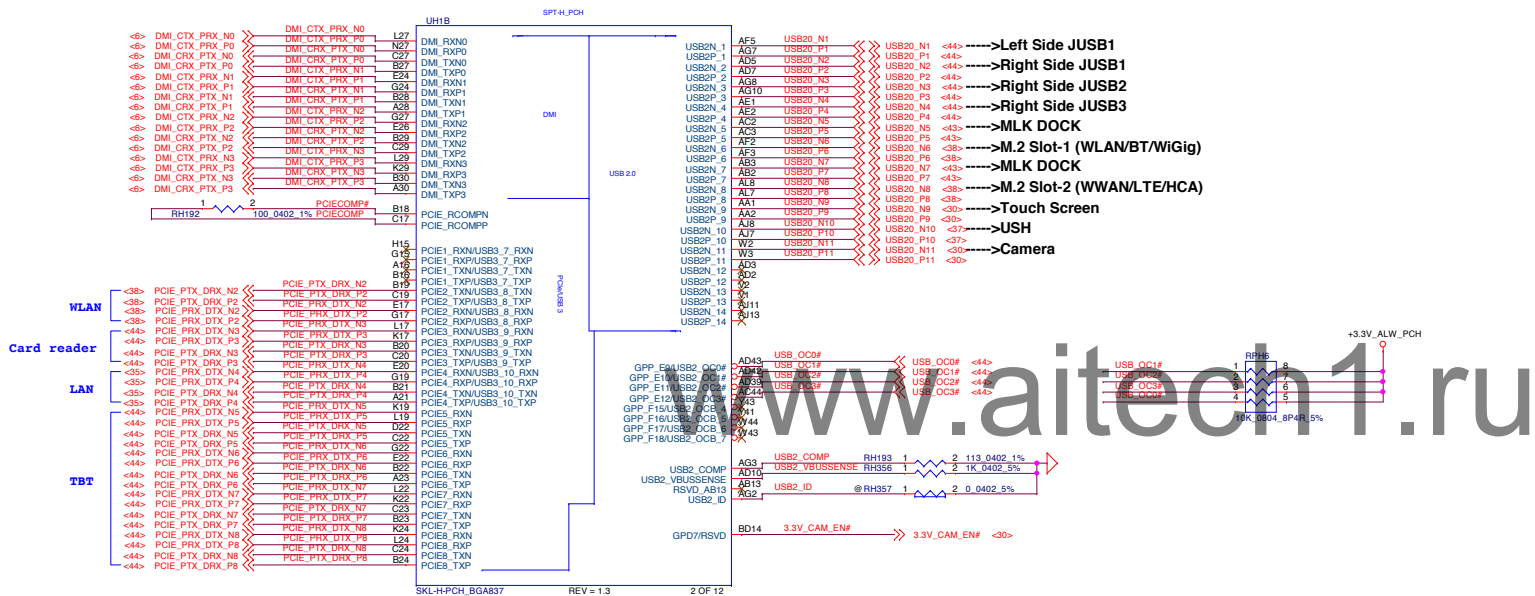
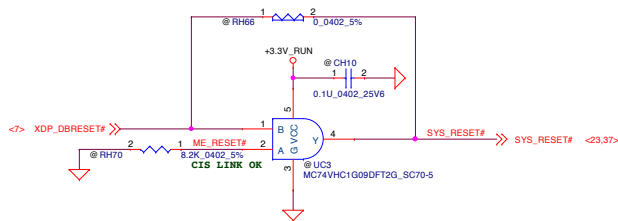
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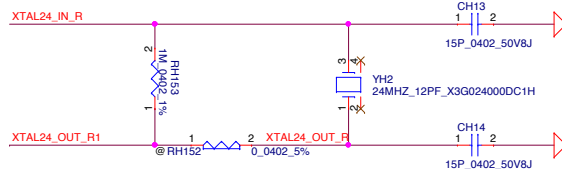
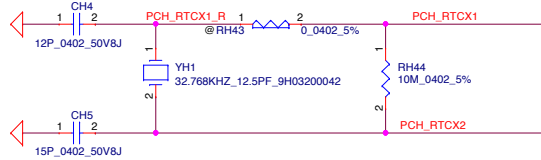
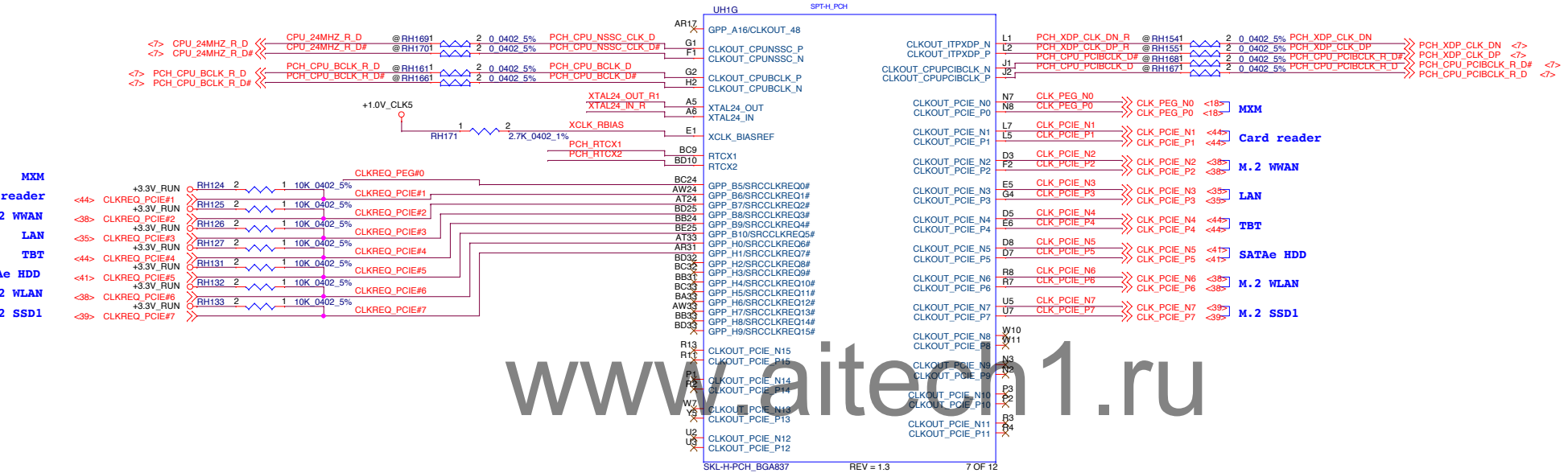
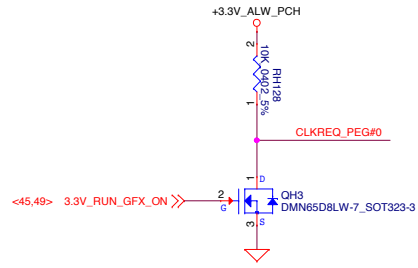
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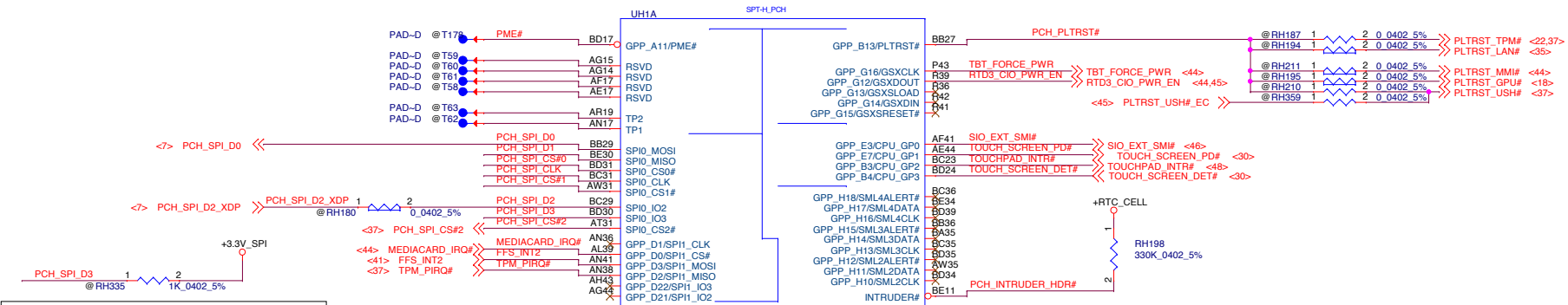
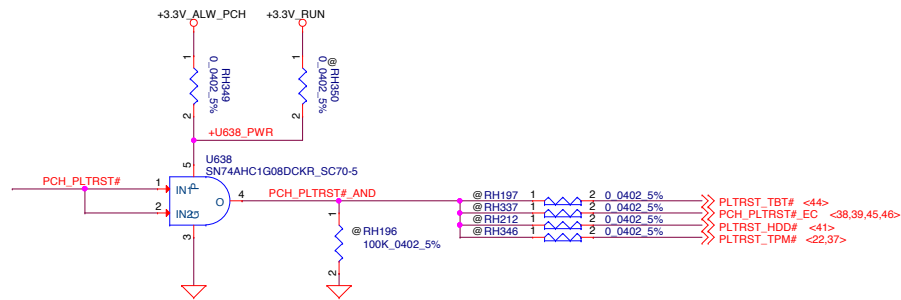
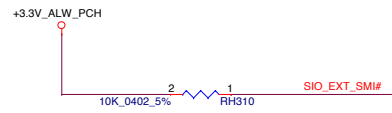
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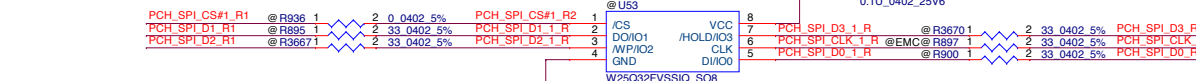
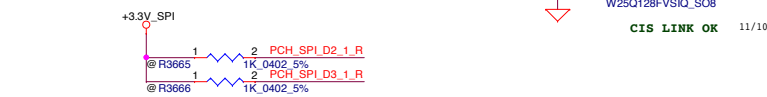
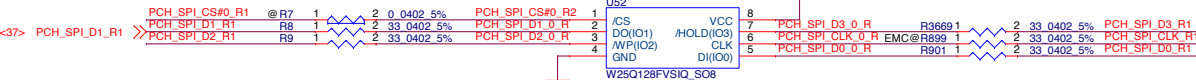
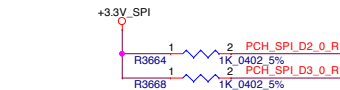
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SKYLAKE PCH-H (3/9)			
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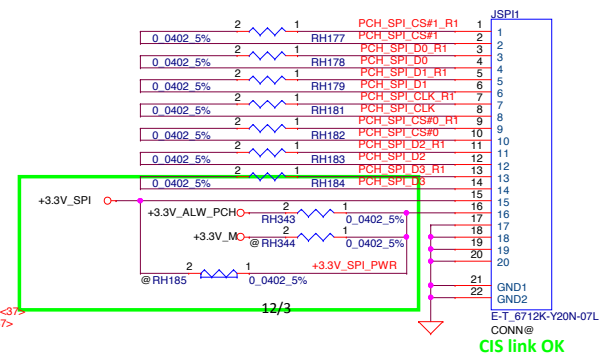
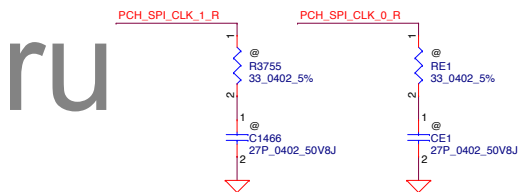
Intel required for pre-ES1/ES2 sample

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200 MIL S08
16MB Flash ROM

200 MIL S08
4MB Flash ROM



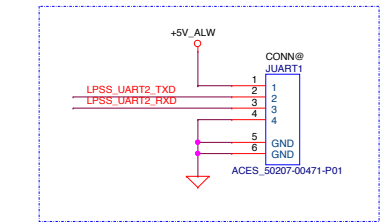
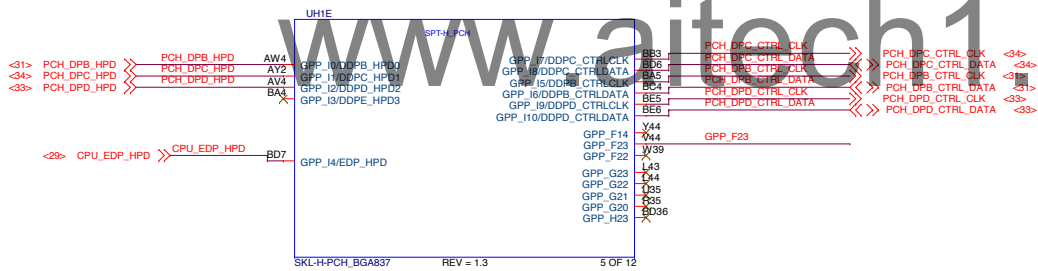
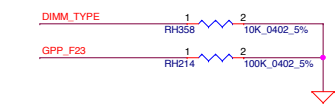
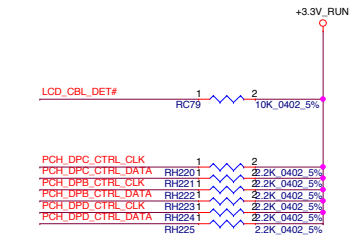
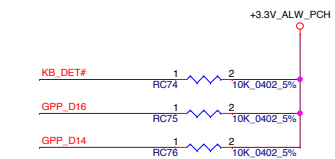
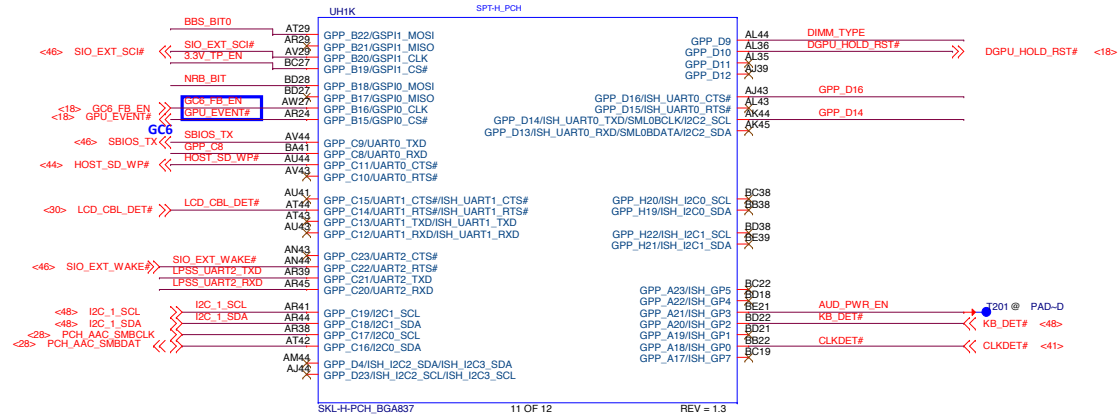
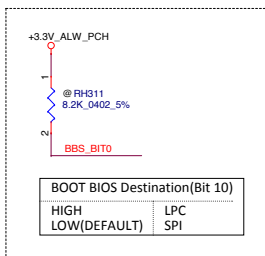
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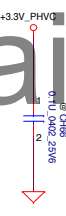
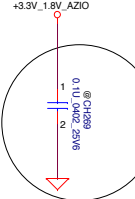
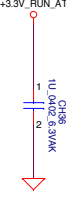
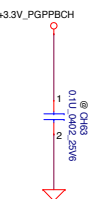
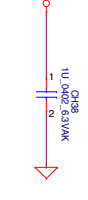
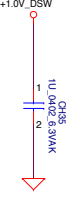
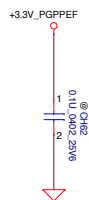
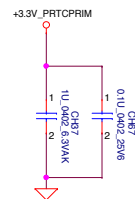
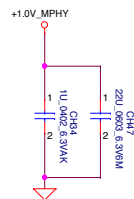
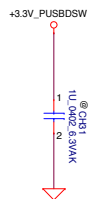
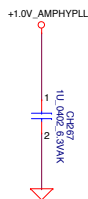
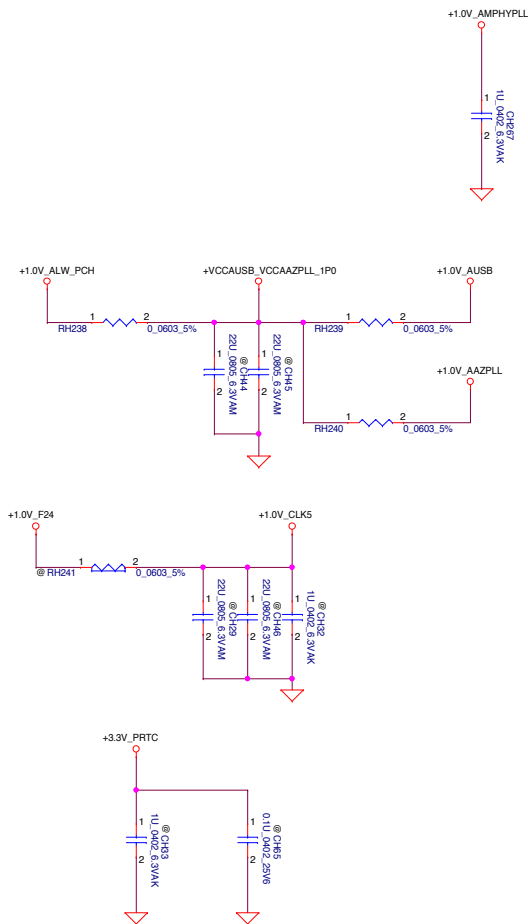
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SKYLAKE PCH-H (4/9)			
LA-C541P			
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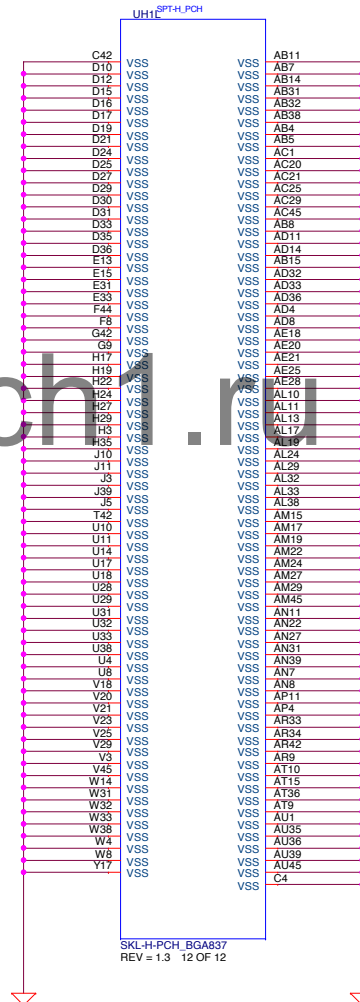
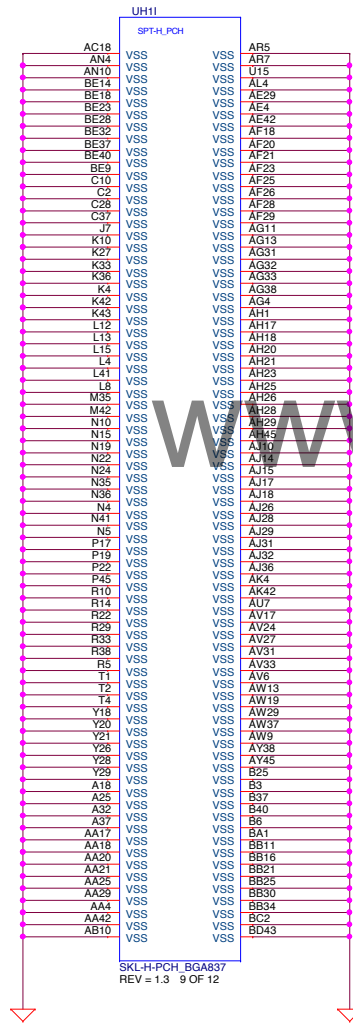


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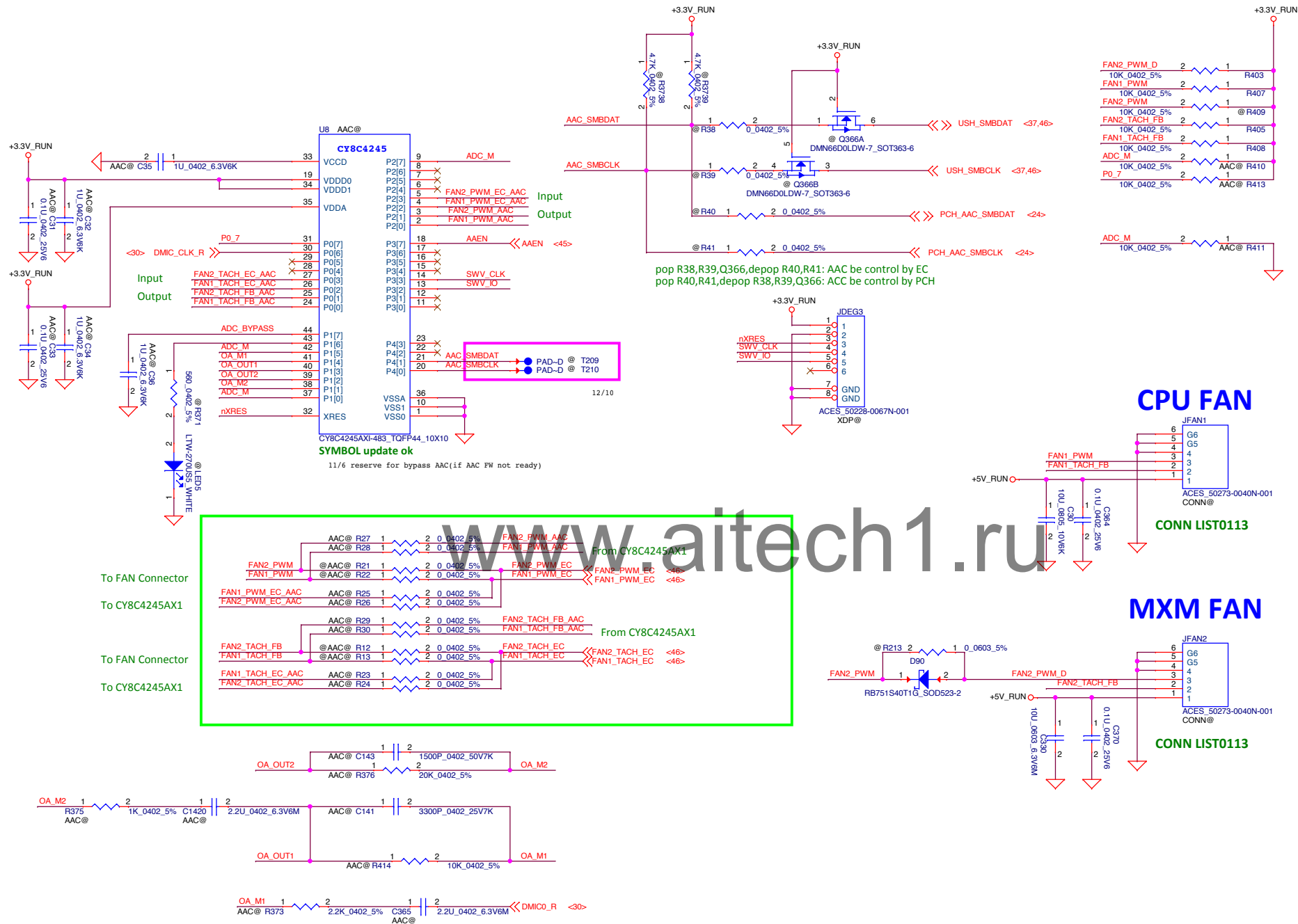


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CPU FAN

CONN LIST0113

MXM FAN

CONN LIST0113

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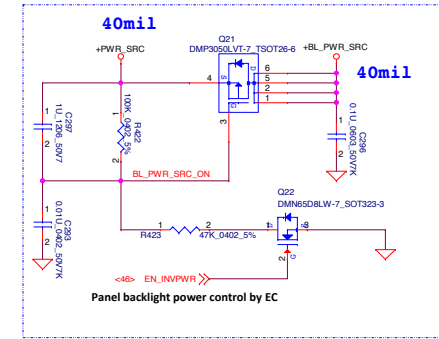
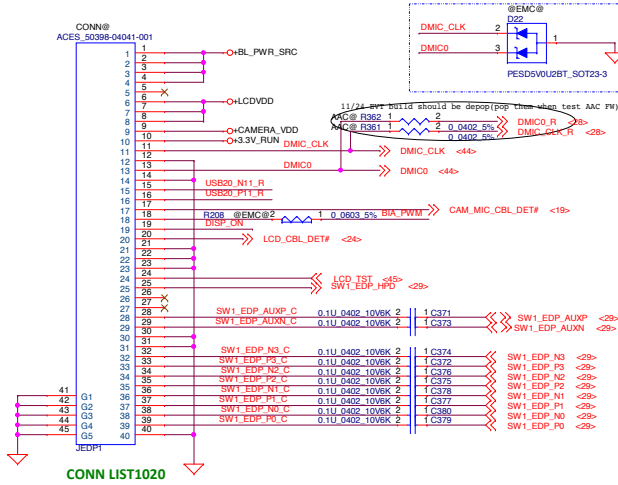
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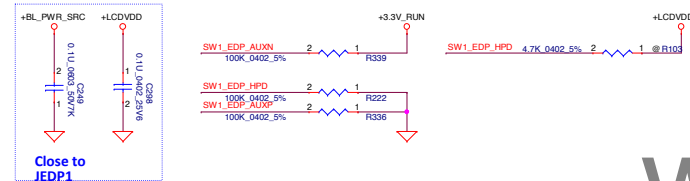
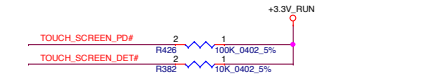
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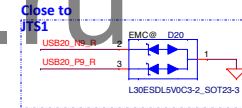
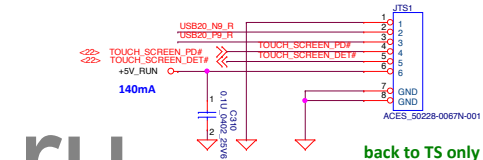
Close to JEDP1



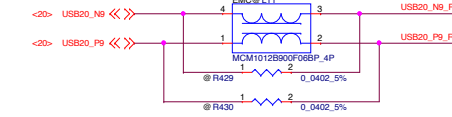
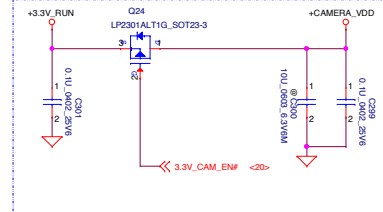
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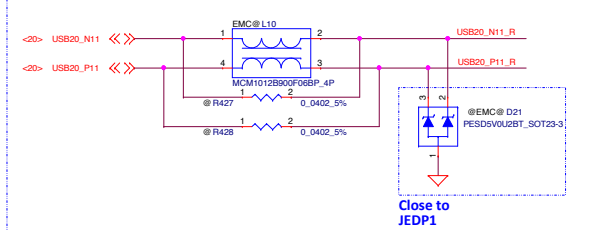
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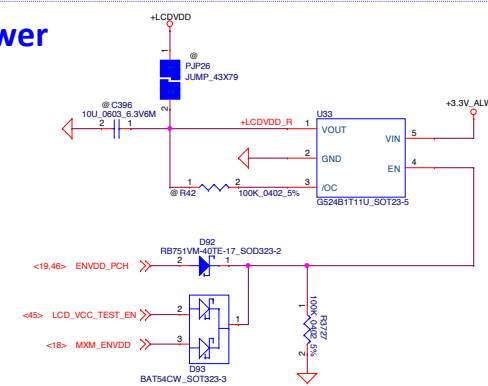
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Camera



LCD Power



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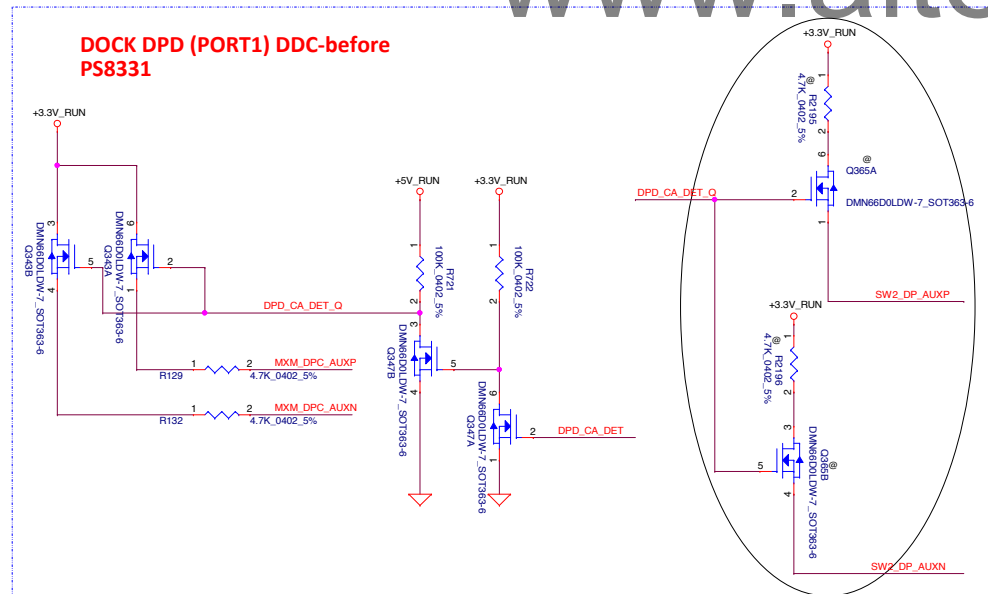
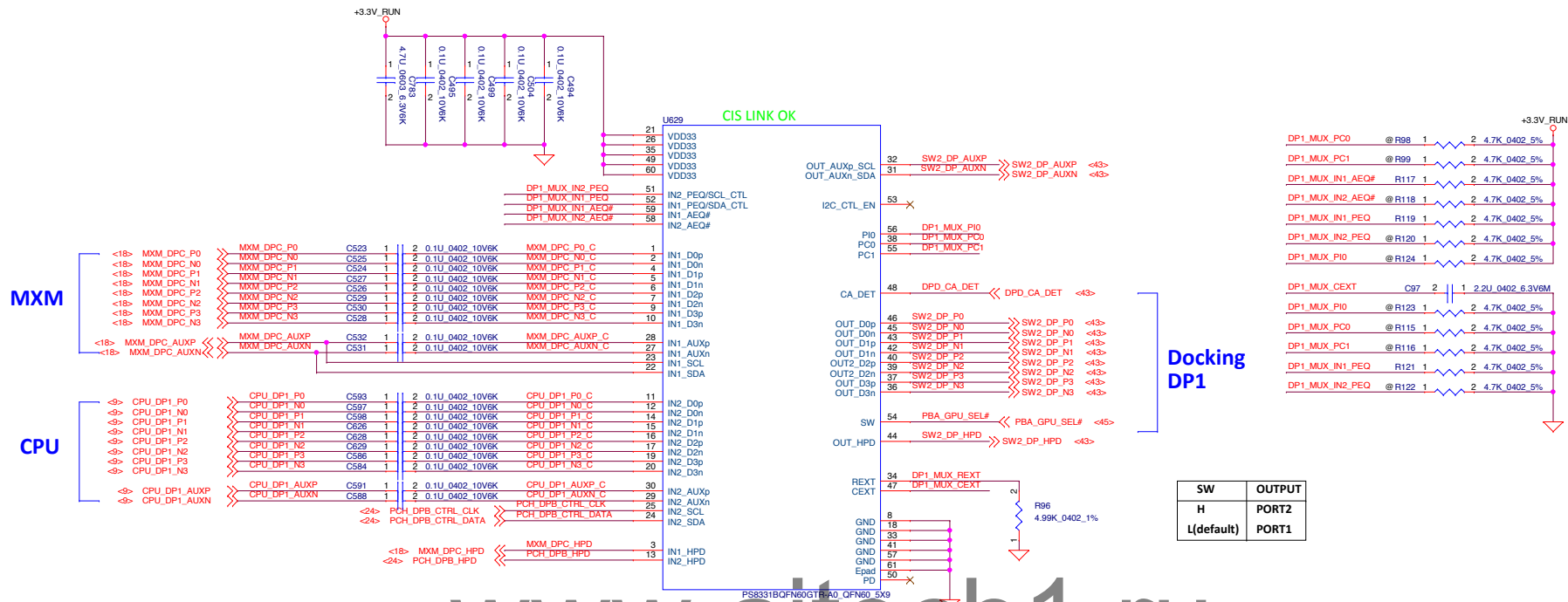
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eDP / CAM / TS

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INy_PEQ = Programmable input equalization levels
 L: default, LED, compensate channel loss up to 11.5dB @ HBR2
 H: HEQ, compensate channel loss up to 14.5dB @ HBR2
 M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

INy_AEQ# = Automatic EQ disable
 L: Automatic EQ enable (default)
 H: Automatic EQ disable

PIO = Auto test enable
 L: Auto test disable & input offset cancellation enable (default)
 H: Auto test enable & input offset cancellation enable
 M: Auto test disable & input offset cancellation disable

PC0 = AUX interception disable
 L: AUX interception enable, driver configuration is set by link training (default)
 H: AUX interception disable, driver output with fixed 800mV and 0dB
 M: AUX interception disable, driver output with fixed 400mV and 0dB

PC1 = Output swing adjustment
 L: default
 H: +20%
 M: -16.7%

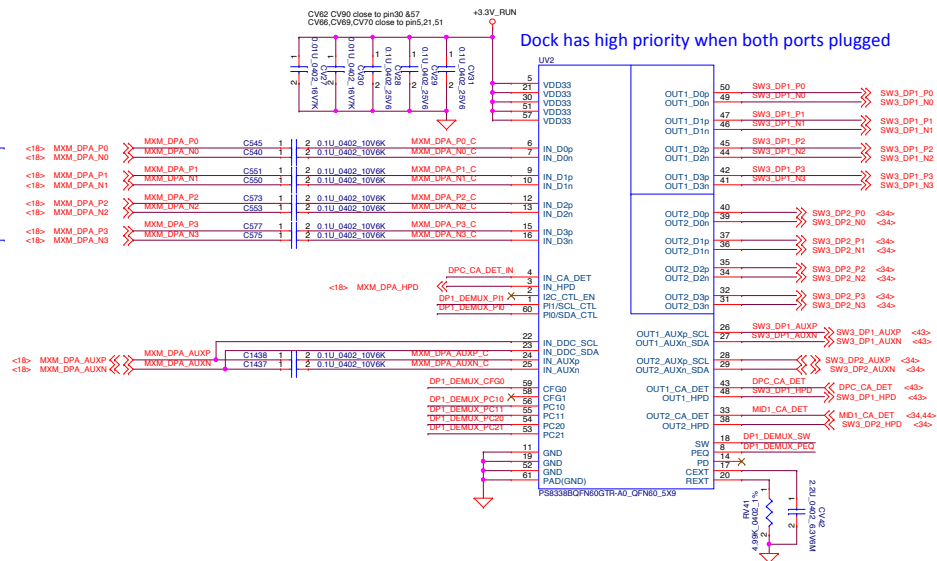
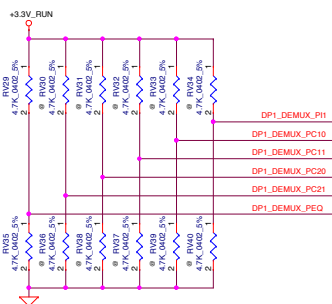
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MXM/CPU MUX(PS8331)



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Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O
For Control Switching Mode (CFG0 = L):
SW = L: Port1 is selected (default)
SW = H: Port2 is selected

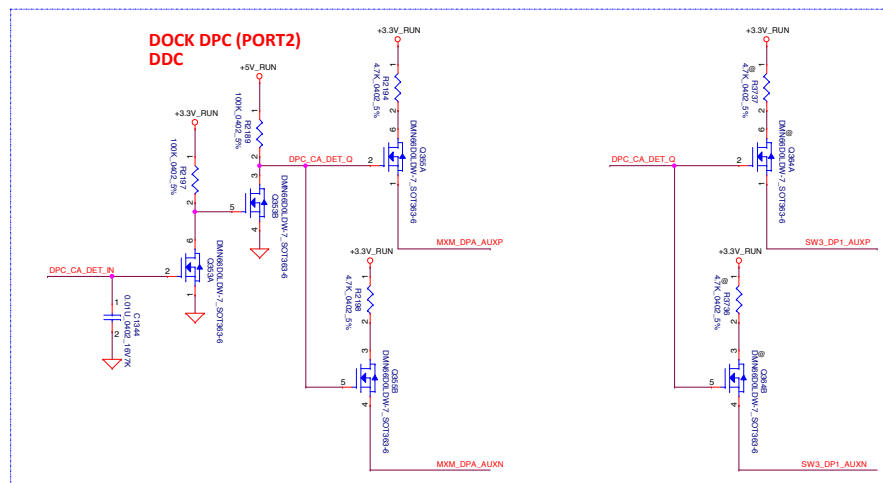
For Automatic Switching Mode (CFG0 = H): (By OUT1_HPD and OUT2_HPD)
SW = L: Port1 has higher priority when both ports are plugged (default)
SW = H: Port2 has higher priority when both ports are plugged

	H	L
CFG0	V	
SW		 V

SW = L: Port1 has higher priority when both ports are plugged (default)
SW = H: Port2 has higher priority when both ports are plugged

SW		V
----	--	---

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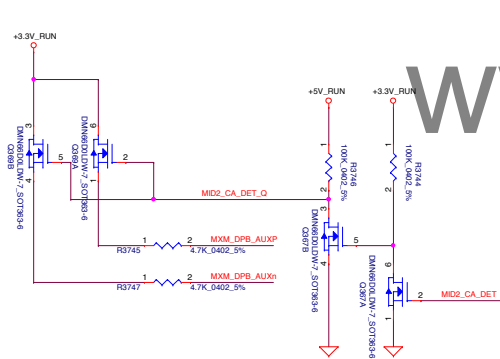
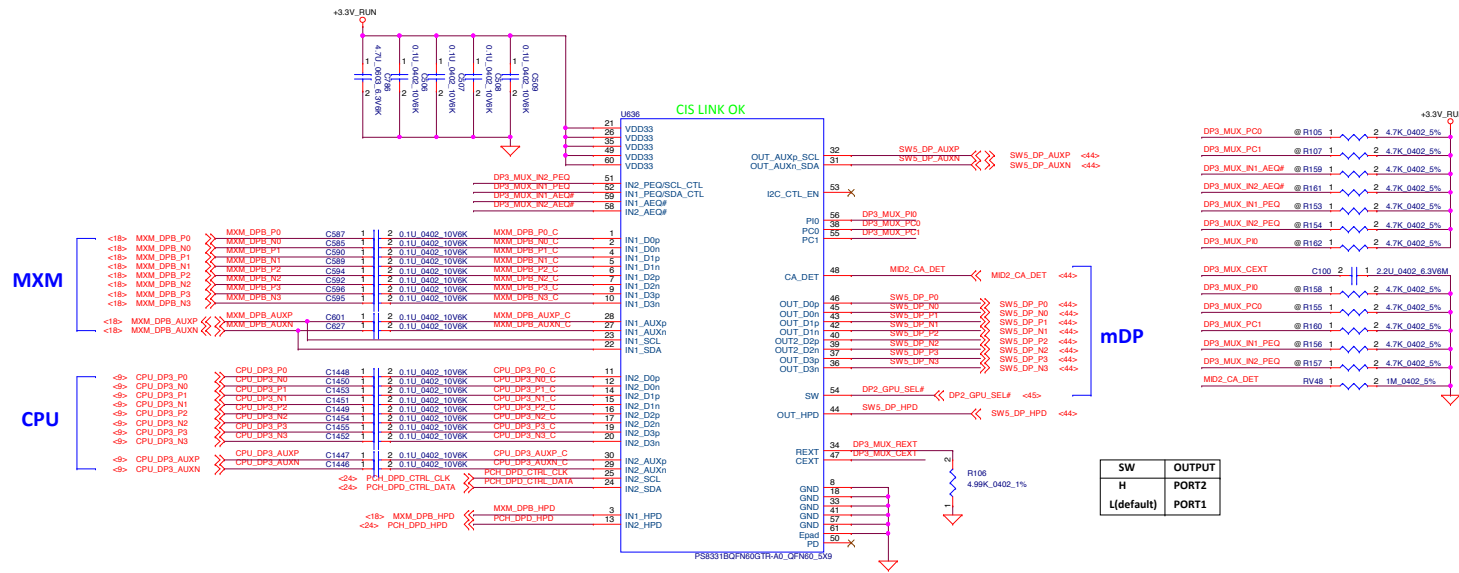


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INy_PEQ = Programmable input equalization levels
 L: Default, LEQ, compensate channel loss up to 11.5dB @ HBR2
 H: HEQ, compensate channel loss up to 14.5dB @ HBR2
 M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

INy_APO# = Automatic EQ disable
 L: Automatic EQ enable (default)
 H: Automatic EQ disable

PIO = Auto test enable
 L: Auto test disable & input offset cancellation enable (default)
 H: Auto test enable & input offset cancellation enable
 M: Auto test disable & input offset cancellation disable

PC0 = AUX interception disable
 L: AUX interception enable, driver configuration is set by link training (default)
 H: AUX interception disable, driver output with fixed 800mV and 0dB
 M: AUX interception disable, driver output with fixed 400mV and 0dB

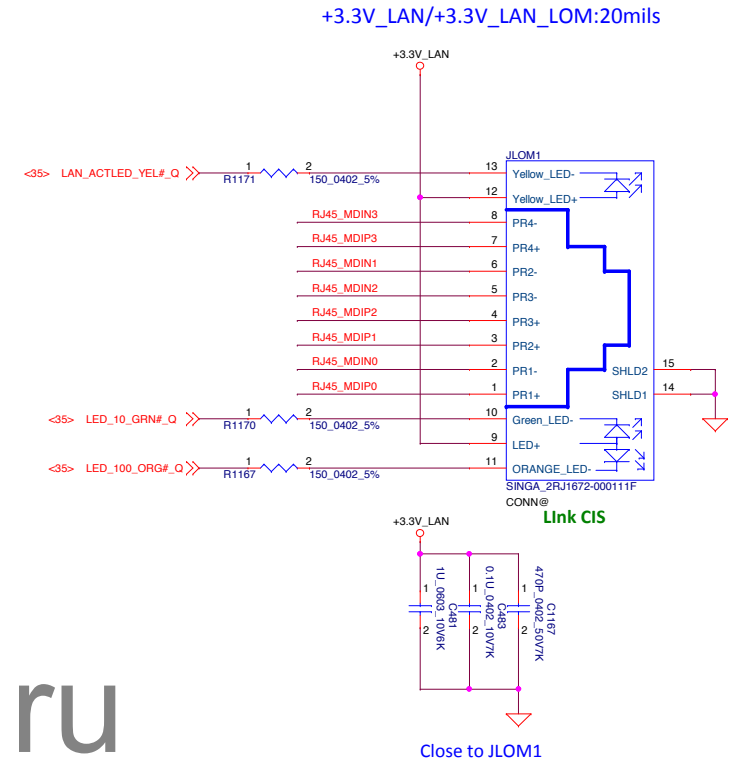
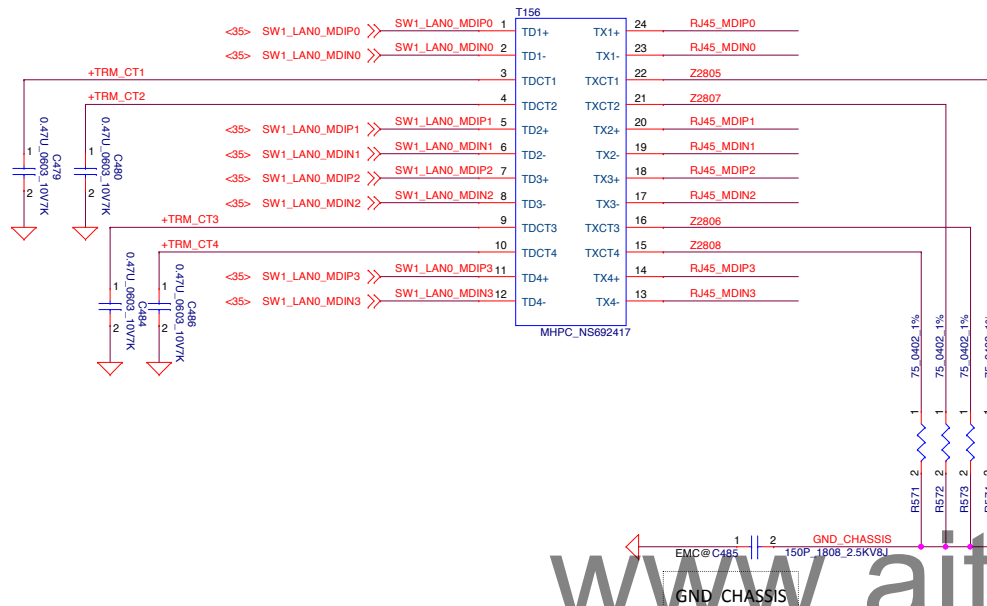
PC1 = Output swing adjustment
 L: default
 H: +20%
 M: -16.7%

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File	DP MUX(PS8331)	Rev	1.0
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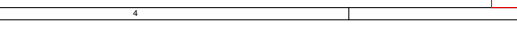
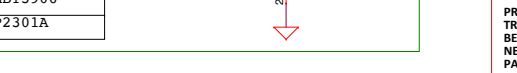
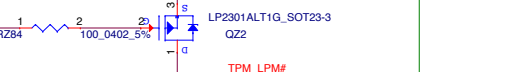
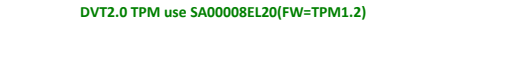
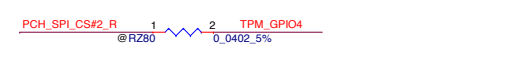
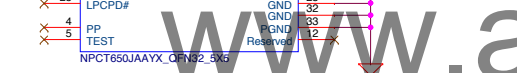
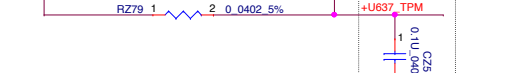
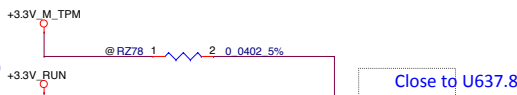
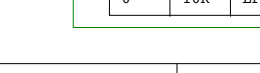
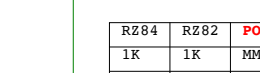
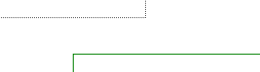
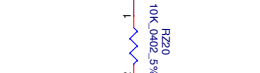
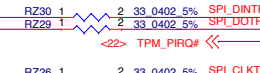
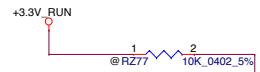
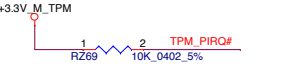
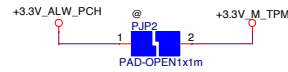
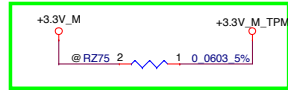
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RJ45

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Size	Document Number	Rev
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power rail option: TPM power rail must same as +3.3V_SPI (SPI ROM)



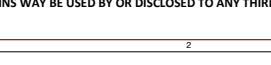
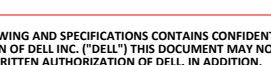
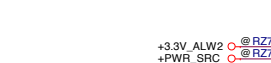
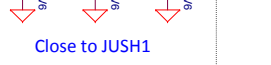
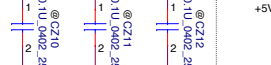
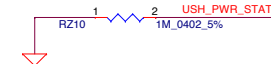
Close to U637.8

Close to U637.1

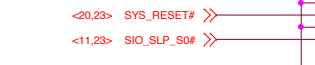
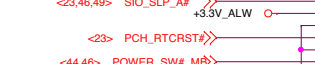
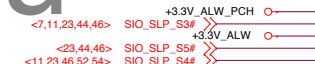
Close to U637.22

Close to U637.14

DVT2.0 TPM use SA00008EL20(FW=TPM1.2)



Check ME about wire to board PN



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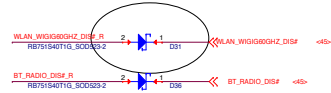
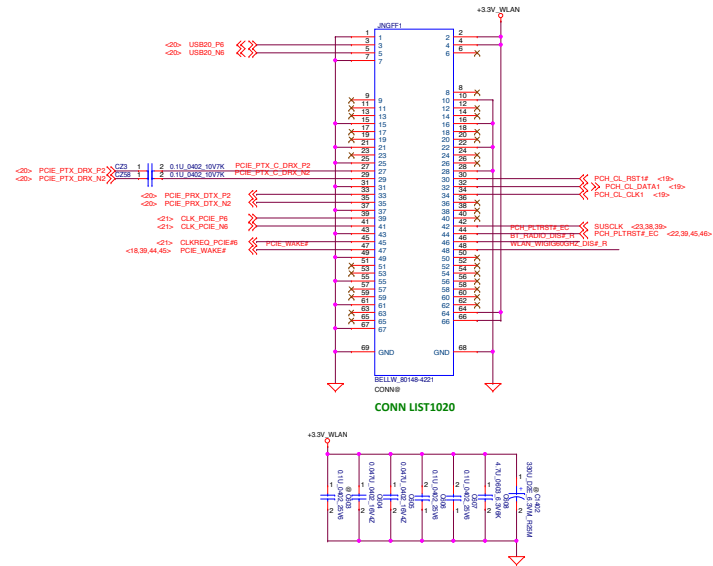


Title			
TPM/USH			
Size	Document Number		Rev
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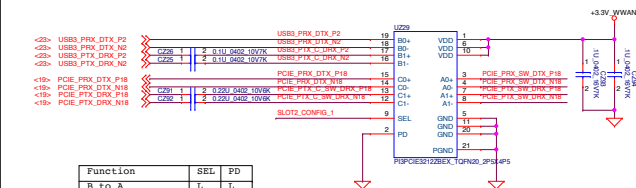
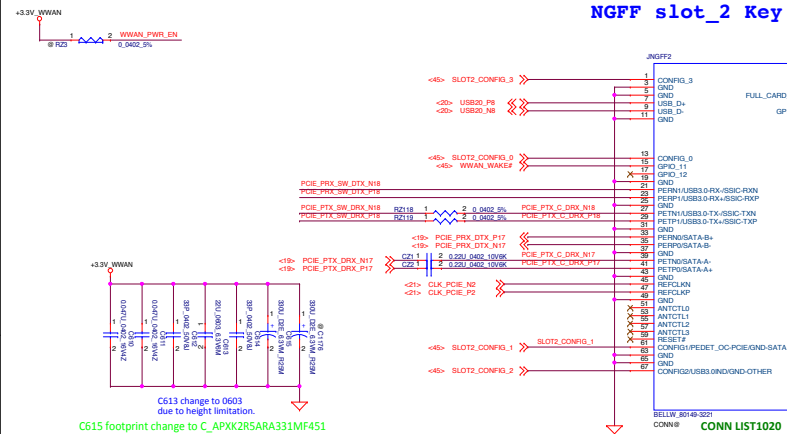
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WLAN/BT

NGFF slot_1 Key A



WWAN/LTE/HCA/Cache
NGFF slot_2 Key B

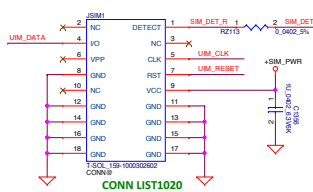


Function	SEL	PD
B to A	L	L
C to A	H	L
All ports Hi-Z, IC power down	X	H

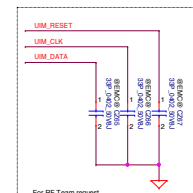
STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	0	0	0	0	SSD-SATA
1	0	1	0	0	SSD-PCIE
8	0	0	1	1	WWAN-USB3
14	1	0	1	1	HCA-PCIE

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SIM Card Push-Push



J5IM1 pin1 (detect)	SIM card detect
0	SIM no present
1	SIM tray present



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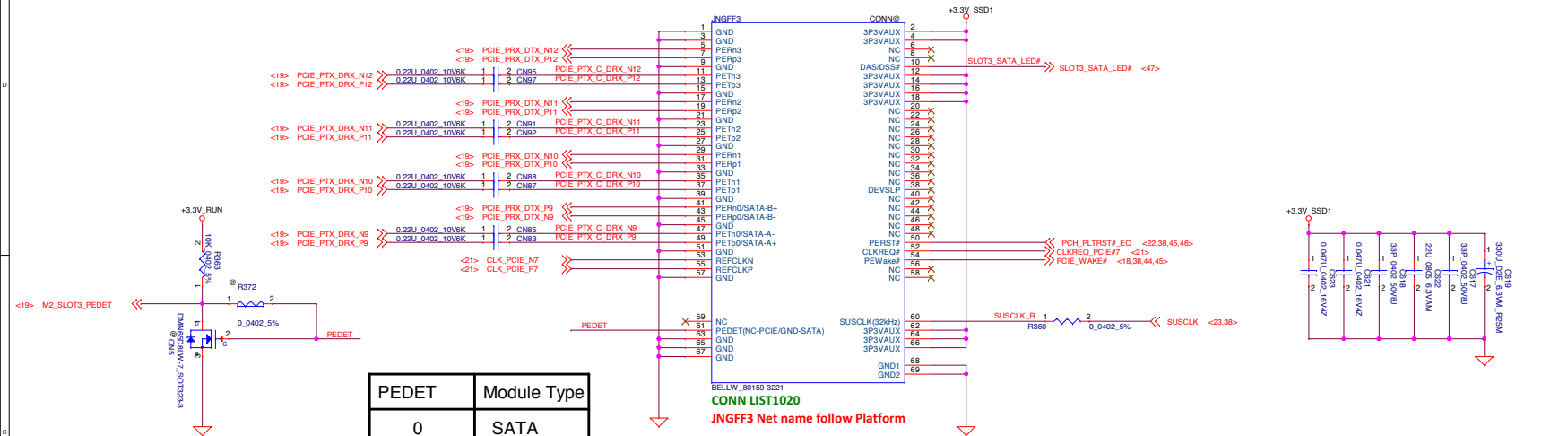
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M.2 Card-1/2

Size	Document Number
------	-----------------

C541P

SSD NGFF slot_3 Key M



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M.2 Card-2/2

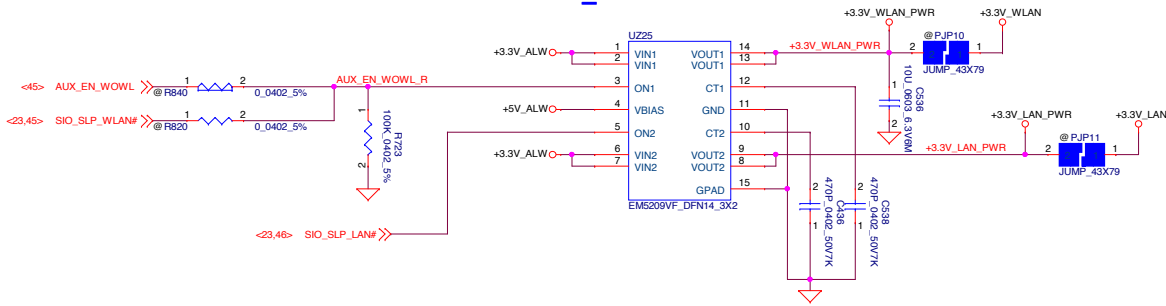
LA-C541P

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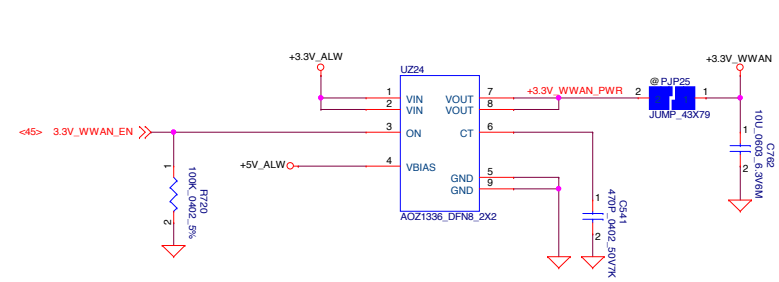
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Power Control for M.2 slot 1. & +3.3V_RUN Source

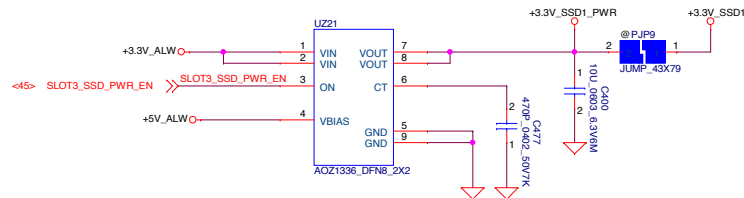


Power Control for M.2 slot 2.



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Power Control for M.2 slot 3. Source



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M.2 Card PWR

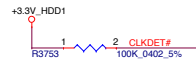
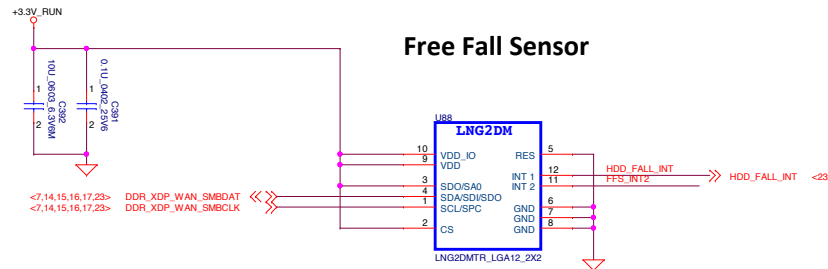
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Size
Date: Monday, August 17, 2015

Document Number
LA-C541P

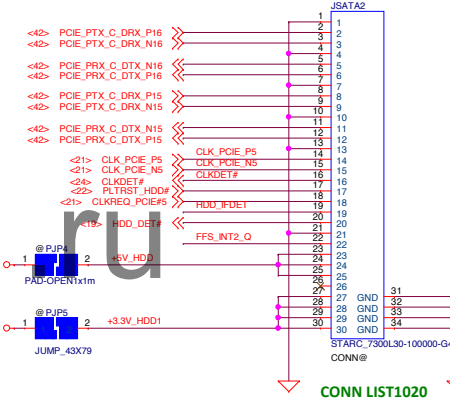
Rev
1.0

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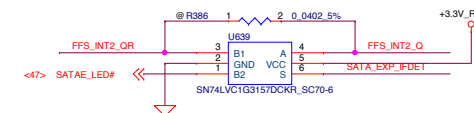
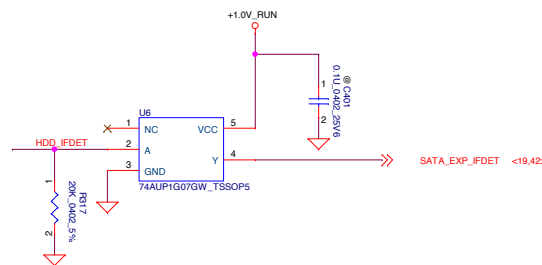
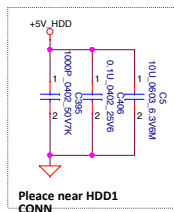
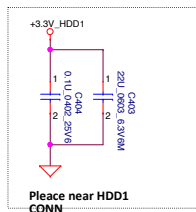
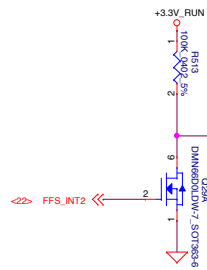
HDD1 CONN



HDD_IFDET	DEVICE interface
0	SATA
1	PCIE

SATA_EXP_IFDET	DEVICE interface
0	SATA
1	PCIE

SATA_EXP_IFDET	channel on
0	A-->B1
1	A-->B2



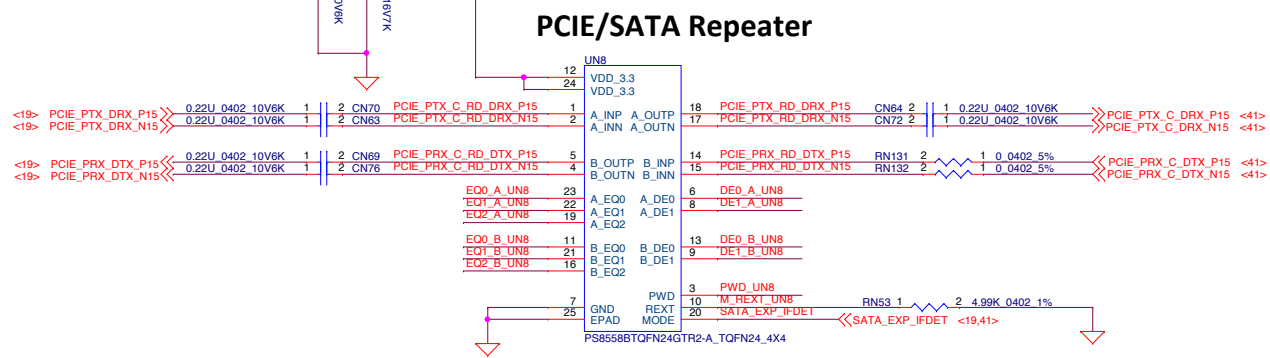
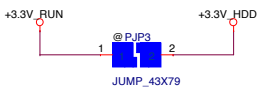
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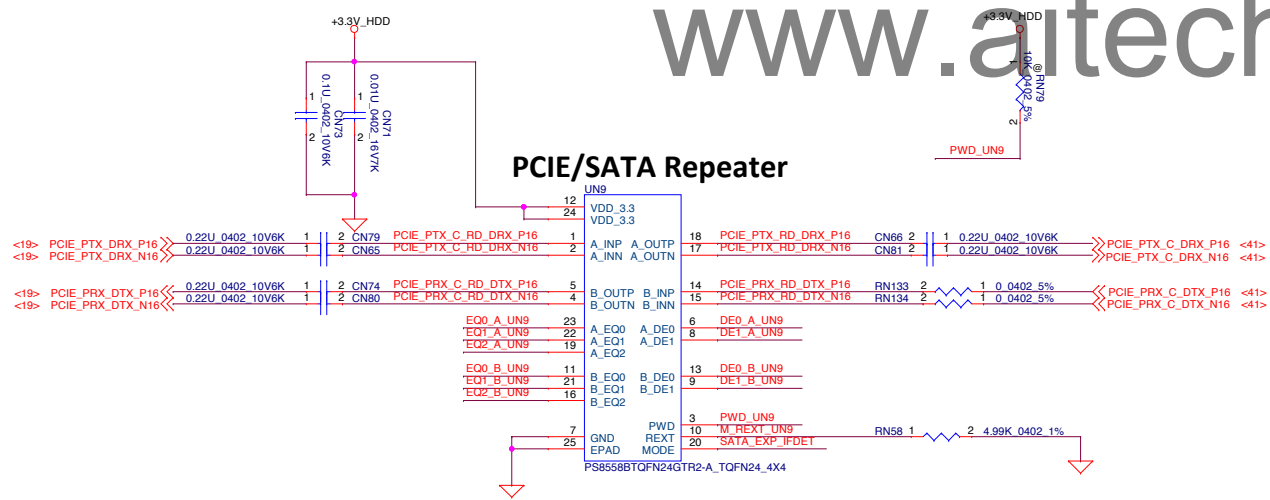
HDD CONN		
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PWD	Funtion
0	Normal mode(Default)
1	Chip power down

SATA_EXP_IFDET	DEVICE interface
0	SATA
1	PCIE



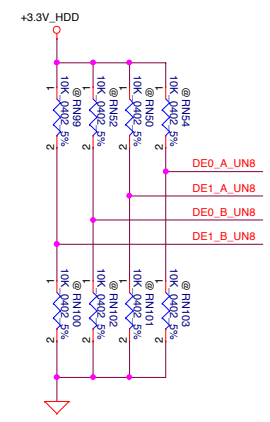
PWD	Funtion
0	Normal mode(Default)
1	Chip power down

SATA_EXP_IFDET	DEVICE interface
0	SATA
1	PCIE

SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

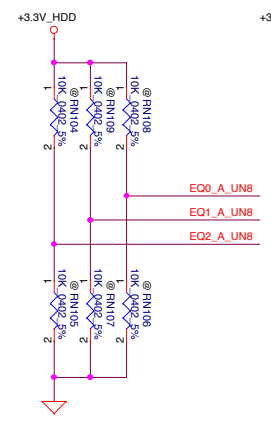
Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

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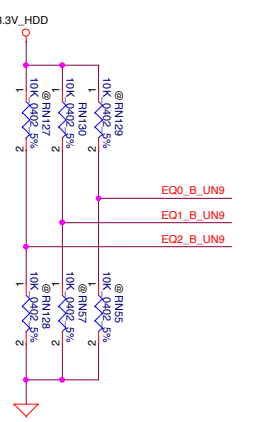
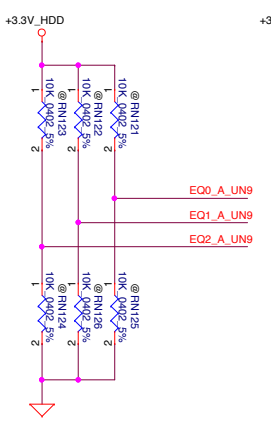
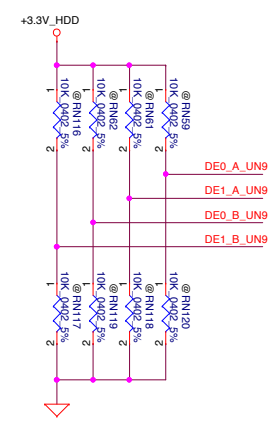
Programmable output de-emphasis level setting for channel A.
A_DE0: internally pulled up at ~150K;
A_DE1 internally pulled down at ~150K

[A_DE1,A_DE0] ==
LL: -7.5dB
HL: -2dB
LH: -3.5dB (default)
HH: -6dB



Equalizer control and program for channel A.
A_EQ0, A_EQ1 and A_EQ2: internally pulled down at ~150K

[A_EQ2,A_EQ1,A_EQ0] ==
LLL: EQ Level1(default)
LHL: EQ Level2
HLL: EQ Level3
HHL: EQ Level4
LHH: EQ Level5
LHH: EQ Level6
HLH: EQ Level7
HHH: EQ Level8

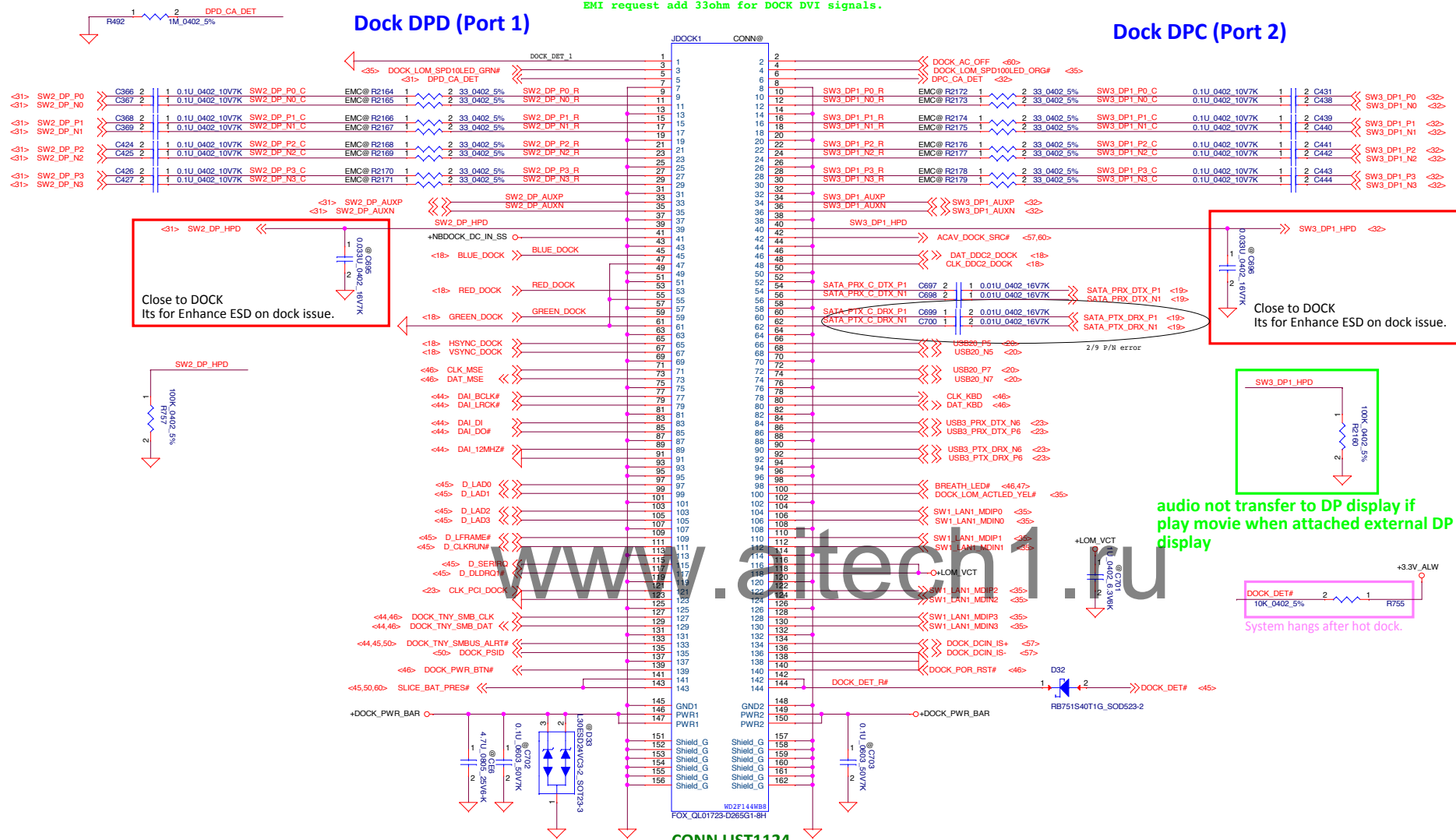


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Title: HDD PCIE/SATA repeater			
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Dock DPD (Port 1)

Dock DPC (Port 2)



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USB/Codec/Card reader IO/B

Display daughter /B

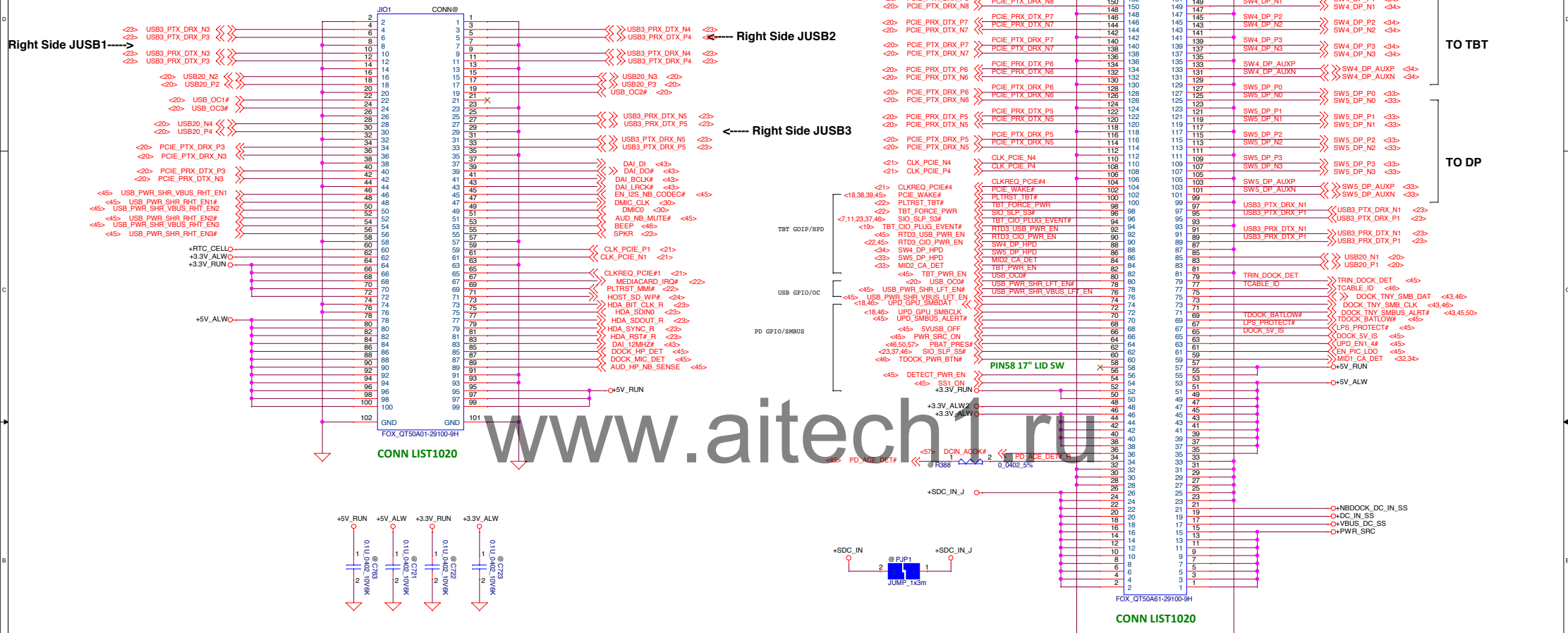
Right Side JUSB1-----

Right Side JUSB2

Right Side JUSB3

TO TBT

TO DP

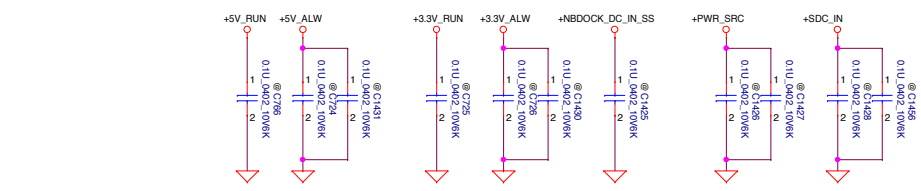
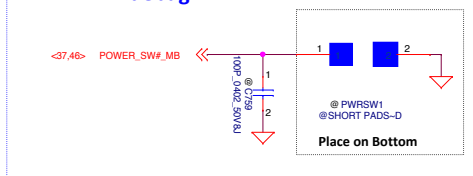
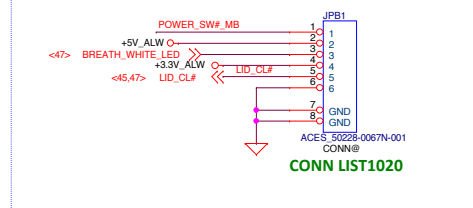


CONN LIST1020

CONN LIST1020

Power Button CONN

Power Switch for debug



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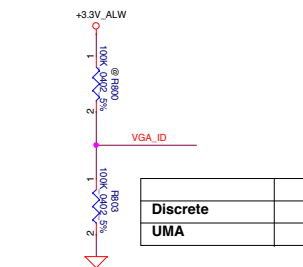
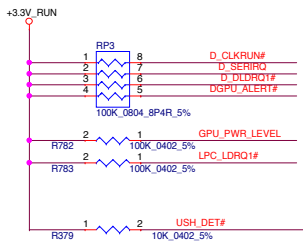
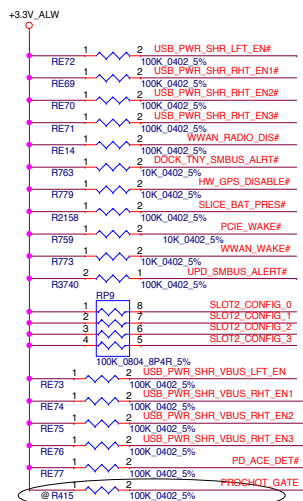
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IO / PWR Button

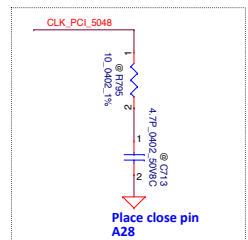
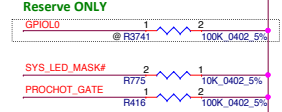
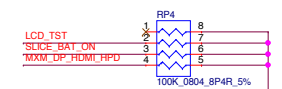
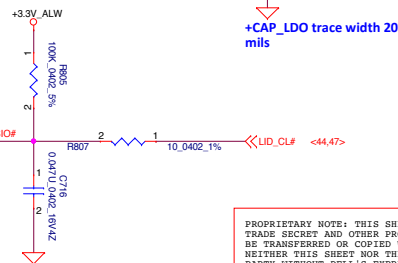
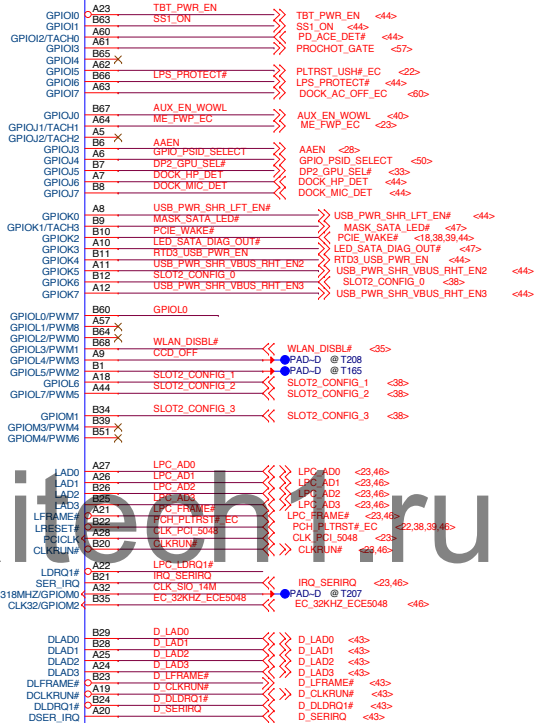
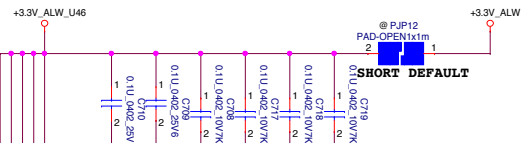
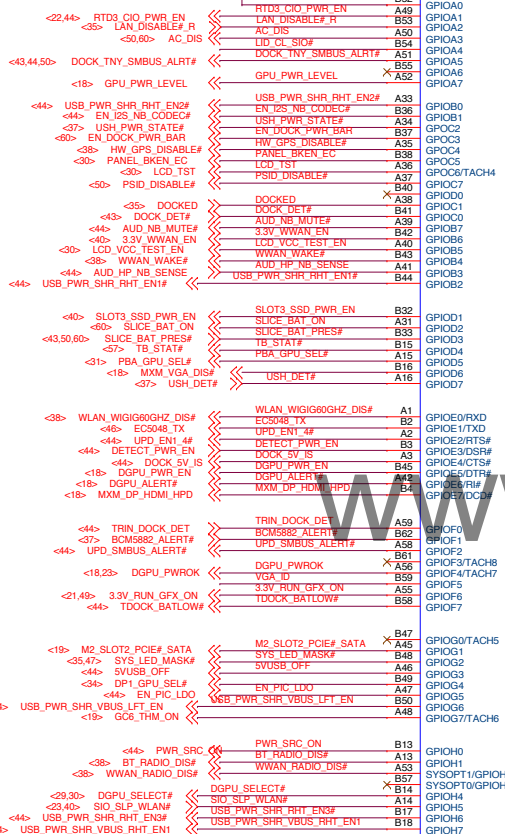
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	VGA_ID
Discrete	0
UMA	1

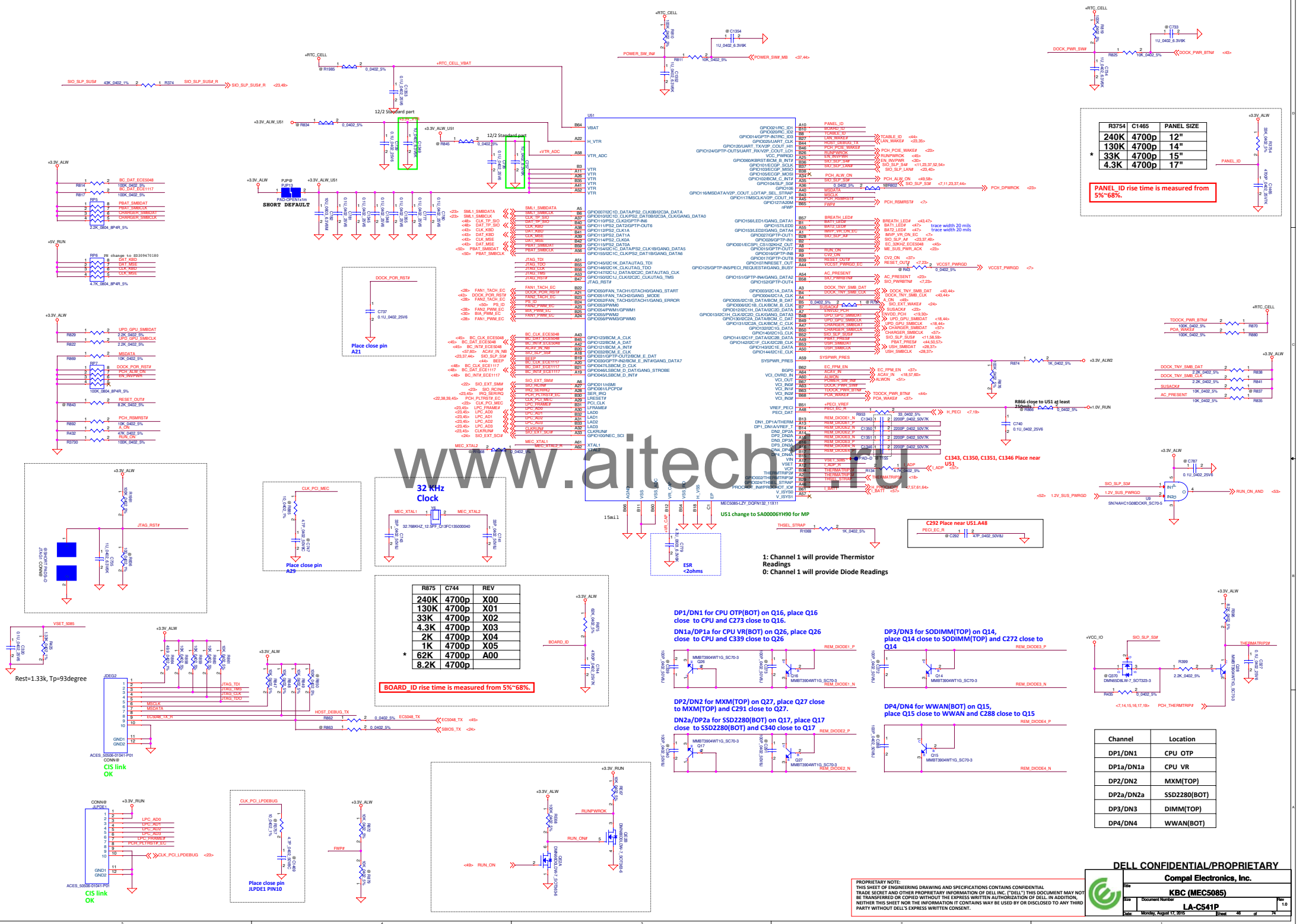


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R3754	C1465	PANEL SIZE
240K	4700p	12"
130K	4700p	14"
33K	4700p	15"
4.3K	4700p	17"

PANEL_ID rise time is measured from 5%-68%.

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R875	C744	REV
240K	4700p	X00
130K	4700p	X01
33K	4700p	X02
4.3K	4700p	X03
2K	4700p	X04
1K	4700p	X05
62K	4700p	A00
8.2K	4700p	

BOARD_ID rise time is measured from 5%-68%.

Channel	Location
DP1/DN1	CPU OTP
DP1a/DN1a	CPU VR
DP2/DN2	MXM(TOP)
DP2a/DN2a	SSD2280(BOT)
DP3/DN3	DIMM(TOP)
DP4/DN4	WWAN(BOT)

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LED Circuit Control Table



3.3V_ALW

@ C778 0.1uF 0.042 25V6

SW 1 2

U58 1H 2

SN74AHC1G08BCKR_SC70-5

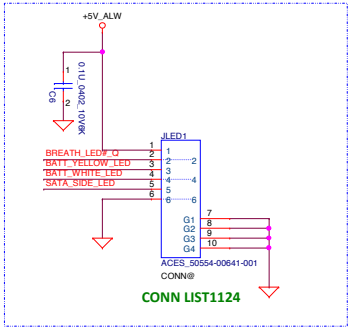
<35,45> SYS_LED_MODULE#

SYS_LED_MASK#

<44,45> LID_CL#

LID_CL#

MASK_BASE_LED#



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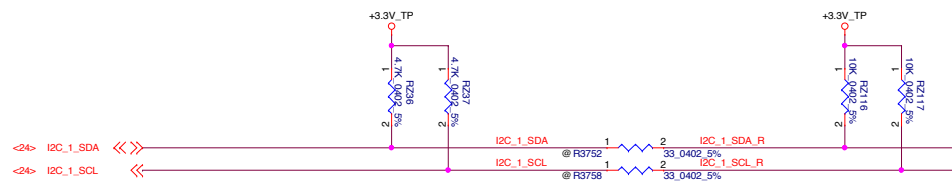
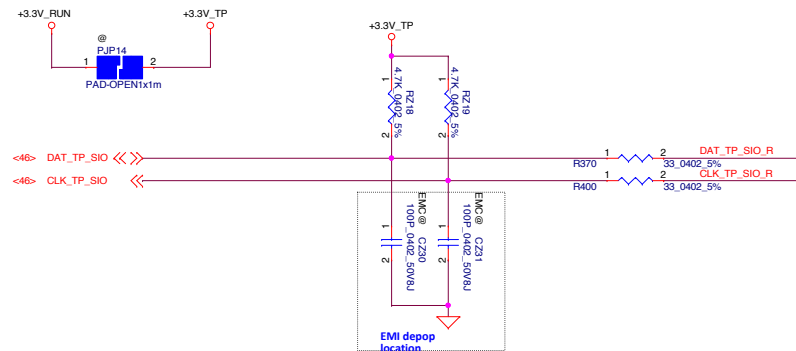
Compal Electronics, Inc.

LED / Screw hole

LA-C541P

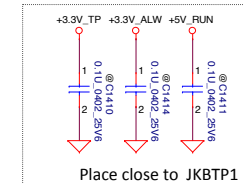
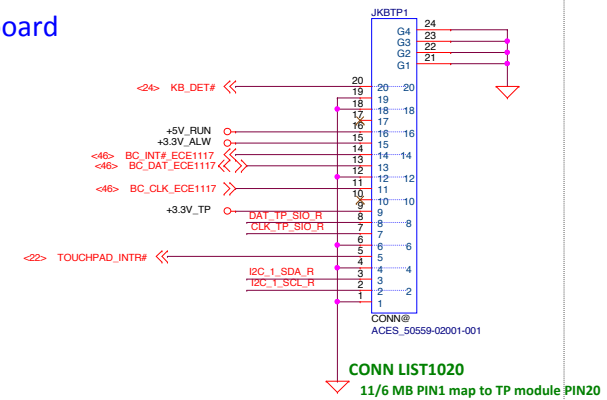
	LA-C541P	1.0
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Touch Pad



pop R3752, R3758 and depop R236, R237 when use I2C_TP

Keyboard



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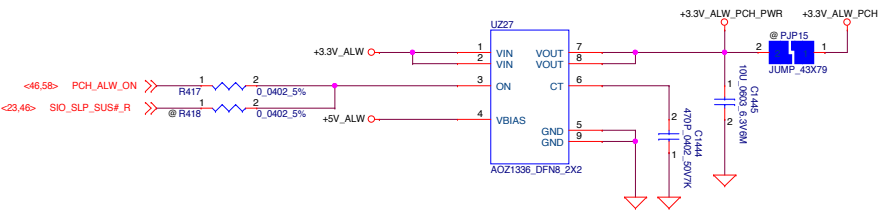
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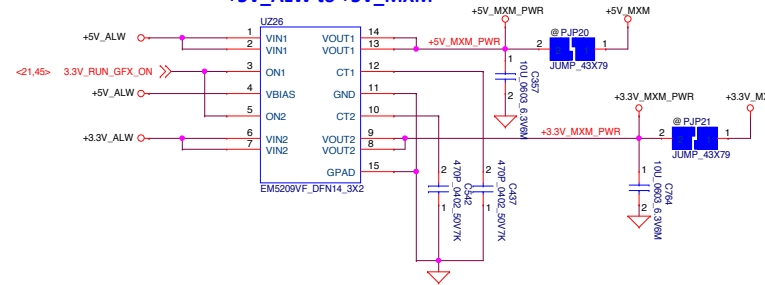
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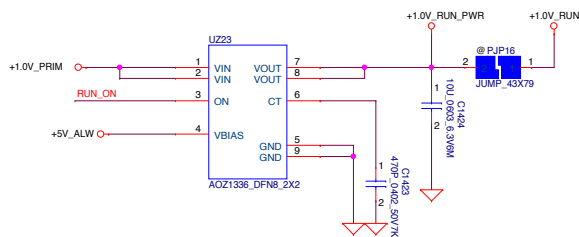
+3.3V_ALW_PCH Source



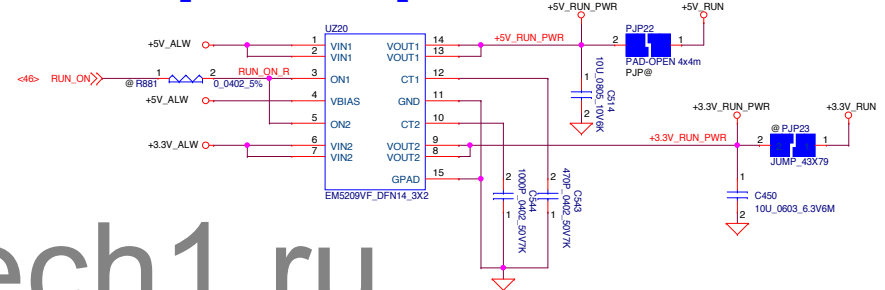
+3.3V_ALW to +3.3V_MXM +5V_ALW to +5V_MXM



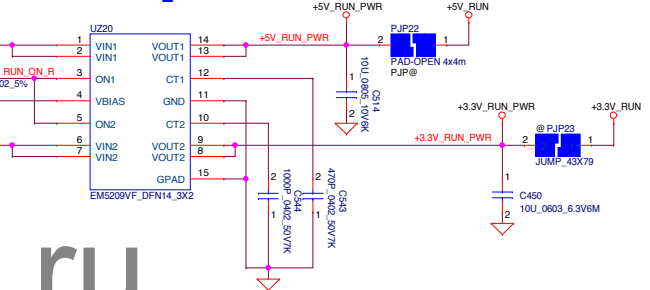
+1.0V_PRIM to +1.0V_RUN



+5V_RUN Source

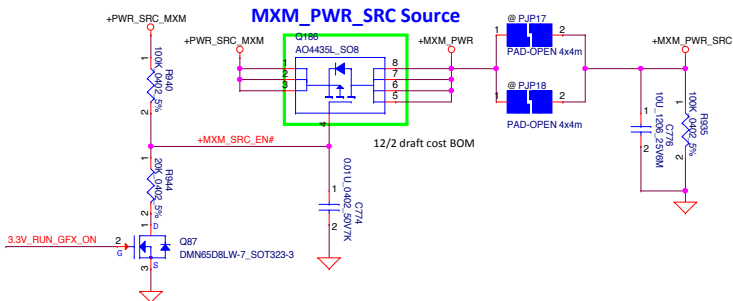


+3.3V_RUN Source

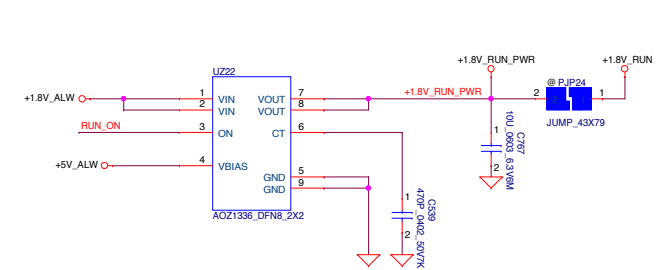


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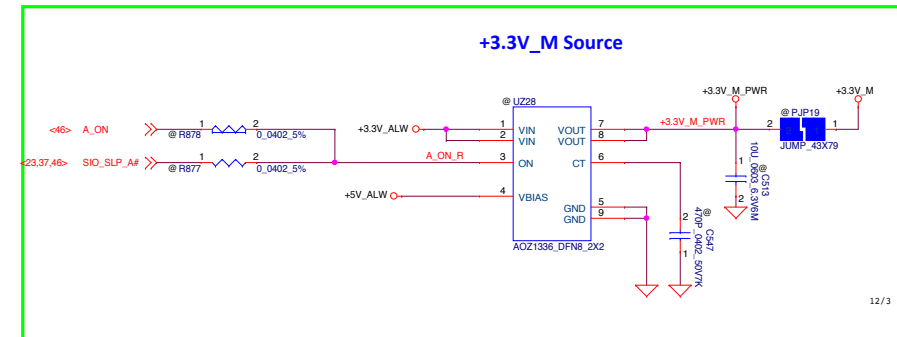
MXM_PWR_SRC Source



+1.8V_RUN Source



+3.3V_M Source



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Power Control

LA-C541P

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EMI Part (47.1)

DVT1.2 change item

+PWR_SRC

ESD Diodes

DVT2.0 combine H42,H44e to one schematic
BOM structure add H42@,H44@

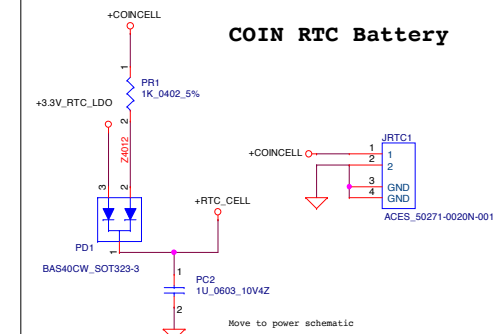
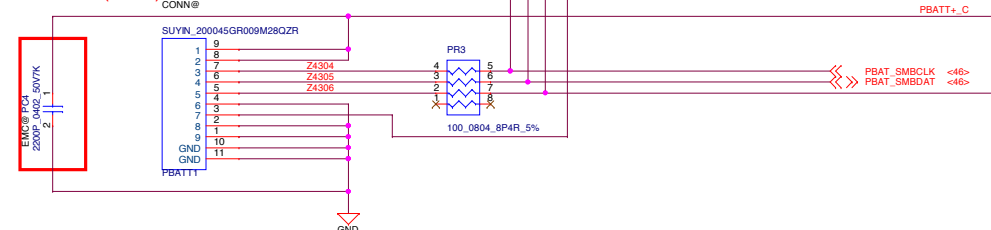
different between H42&H44e

ESD (47.2)

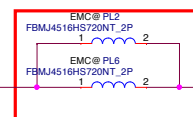
DVT2.1 change item

X-build change item

COIN RTC Battery

Primary Battery Connector
EMI Part (47.1)

EMI Part (47.1)



+3.3V_ALW

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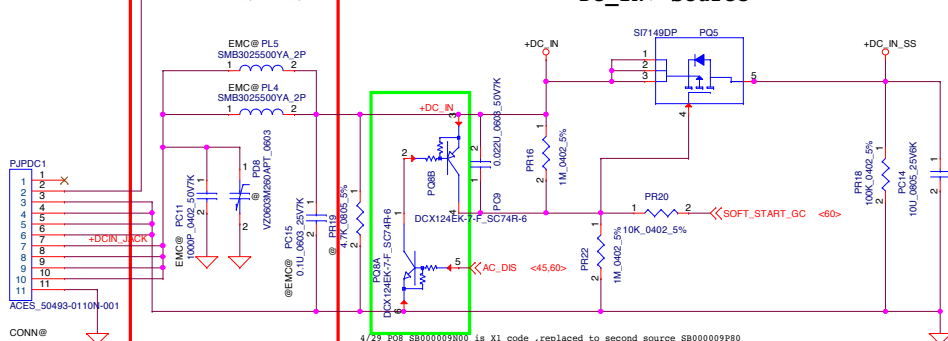
EMI Part (47.1)



6/8 add diode for ESD team Matt request

EMI Part (47.1)

DC_IN+ Source



4/29 PDI SB0000059800 is X1 code ,replaced to second source SB000009P80

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+PWR_SRC

EMI Part (35.33)

+1.2V_MEN_P

EMI Part (35.33)

1.2Volt +/- 5%
TDC: 7.5 A
Peak Current: 11 A
OCP current: 13.2A
Rds(on): 3.5m ohm(max)
Choke DCR 7.4mohm(max)

Mode	S3	S5	+1.35V_MEN	+V_DDR_REF	+0.675V_P
S5	L	L	off	off	off
S3	L	H	on	on	off(Hi-Z)
S0	H	H	on	on	on

0.6Volt +/- 5%
TDC 1.575A
Peak Current 2.25A

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FB sense trace

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Compal Electronics, Inc.	
1.2VP/0.6VSP	
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+PWR_SRC

+3.3V_ALW

+3.3V_ALW

+VCC_IO

TDC 3.85A

Peak Current 5.5 A

OCF Current 8 A

TYP MAX
Choke DCR 13.0mohm, 14.0mohm

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+VCC_IOP

@ PJP300

PAD-OPEN 43x118

+VCC_IOP

proximal

PR311 0 ohm PR314 10 ohm PR316 10 ohm

remote

PR311 10 ohm PR314 0 ohm PR316 0 ohm

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Title

+VCC_IO 0.95V

Size

Document Number

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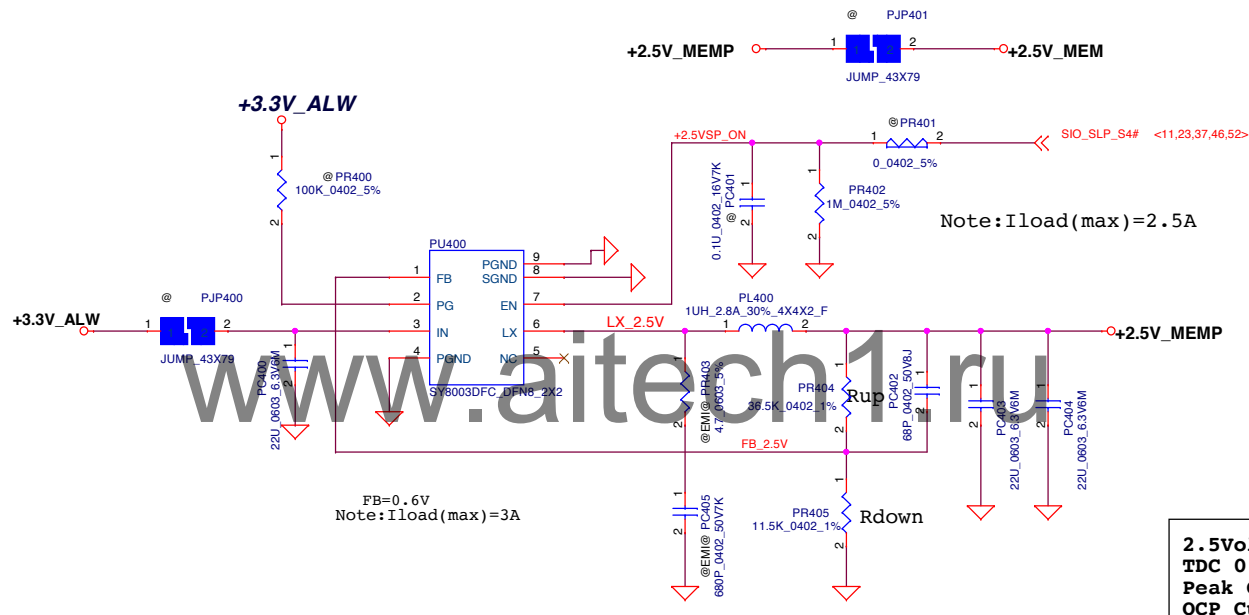
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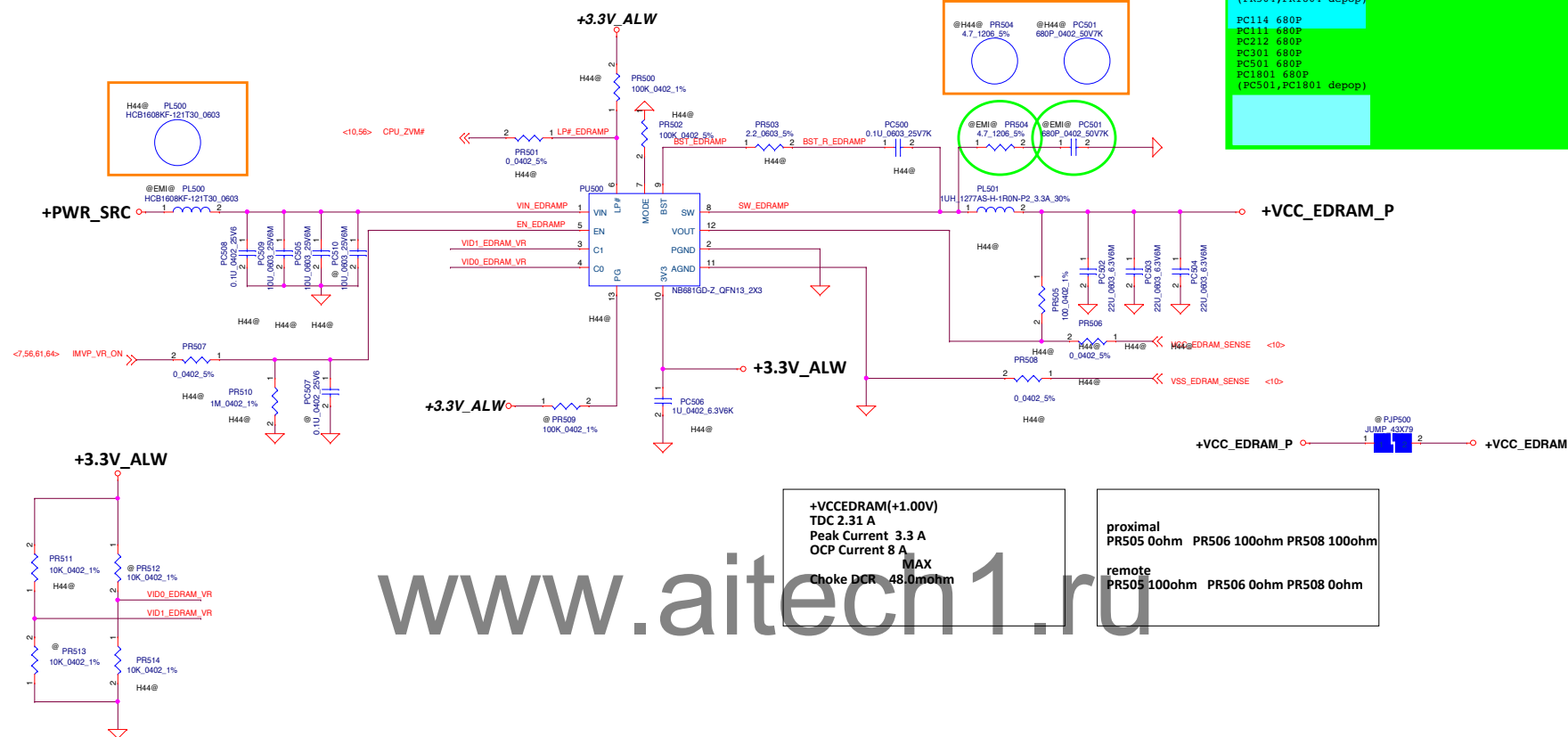


Note:
 When design Vin=5V, please stuff snubber
 to prevent Vin damage

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+2.5V_MEM			
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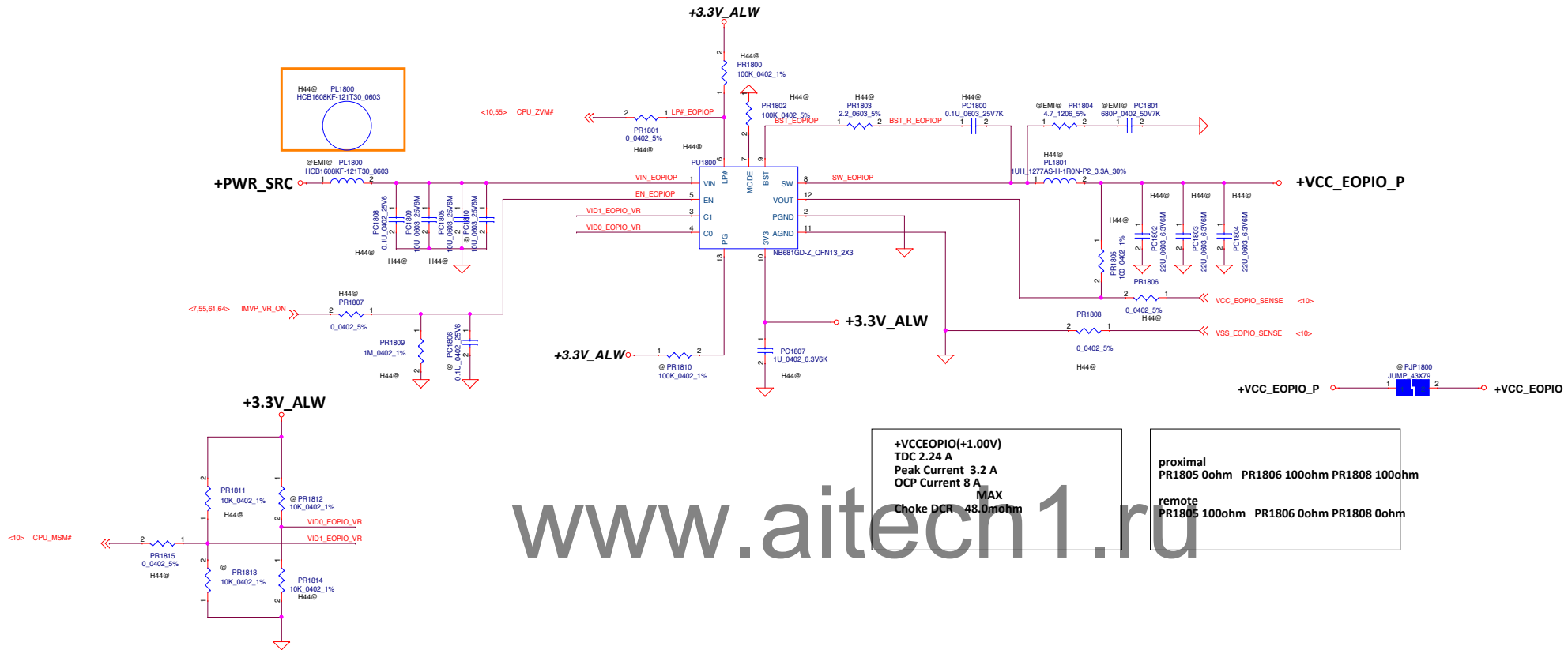
+VCCEDRAM, 1V

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+VCC_EOPIO, 1V

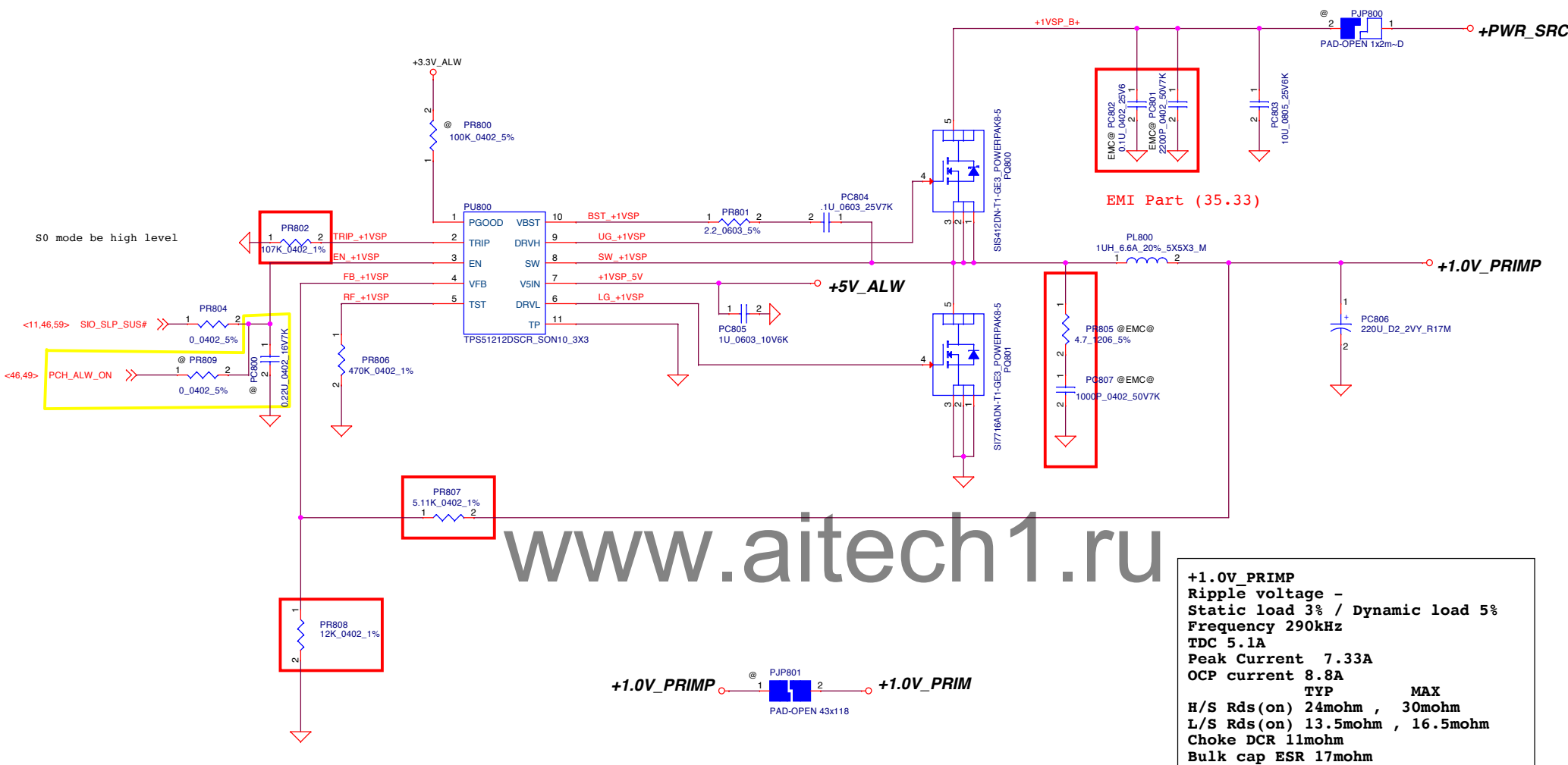
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+1.0V_PRIMP
 Ripple voltage -
 Static load 3% / Dynamic load 5%
 Frequency 290kHz
 TDC 5.1A
 Peak Current 7.33A
 OCP current 8.8A

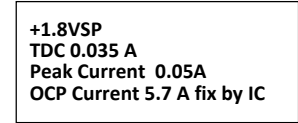
	TYP	MAX
H/S Rds(on)	24mohm	30mohm
L/S Rds(on)	13.5mohm	16.5mohm
Choke DCR	11mohm	
Bulk cap ESR	17mohm	

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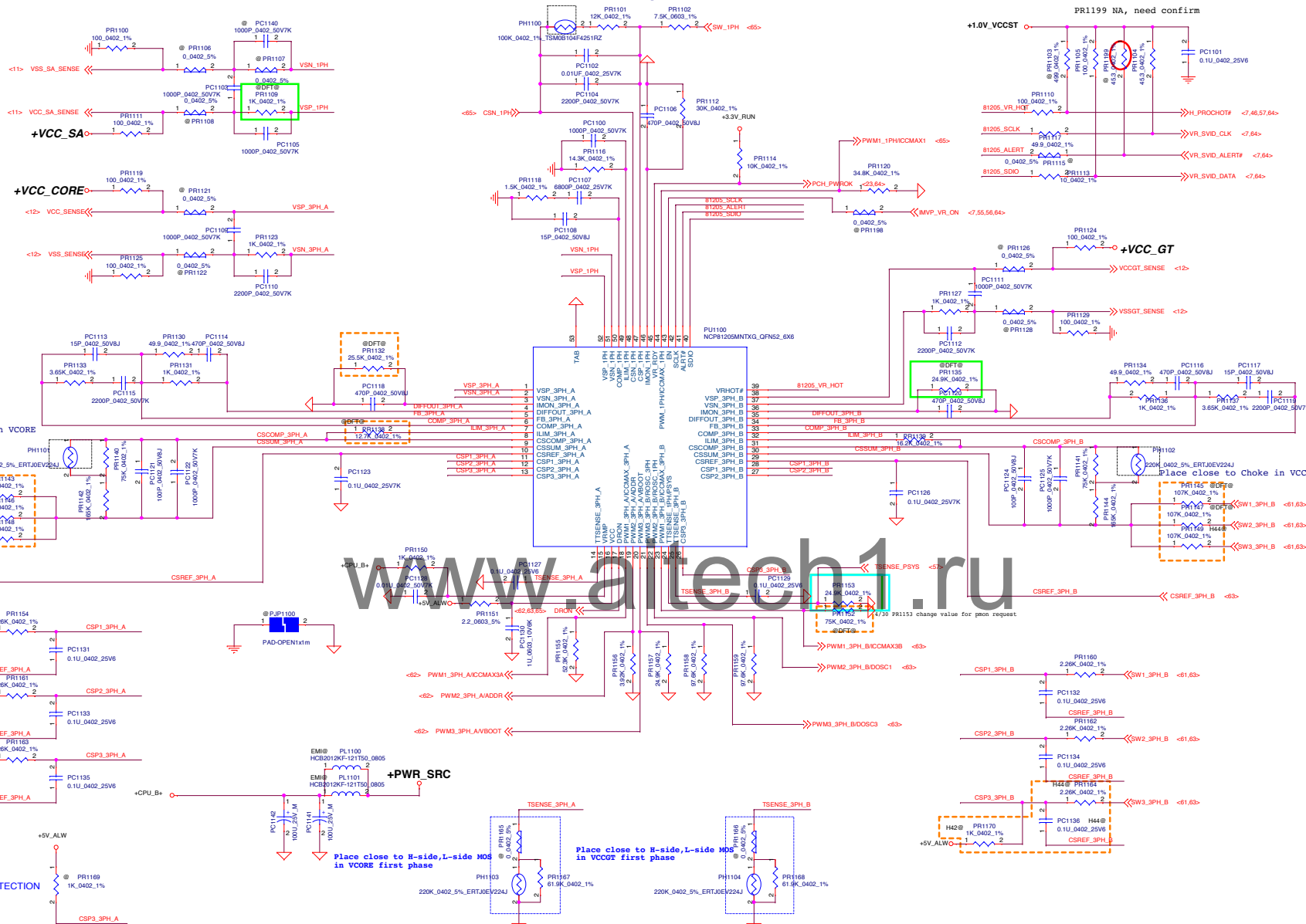
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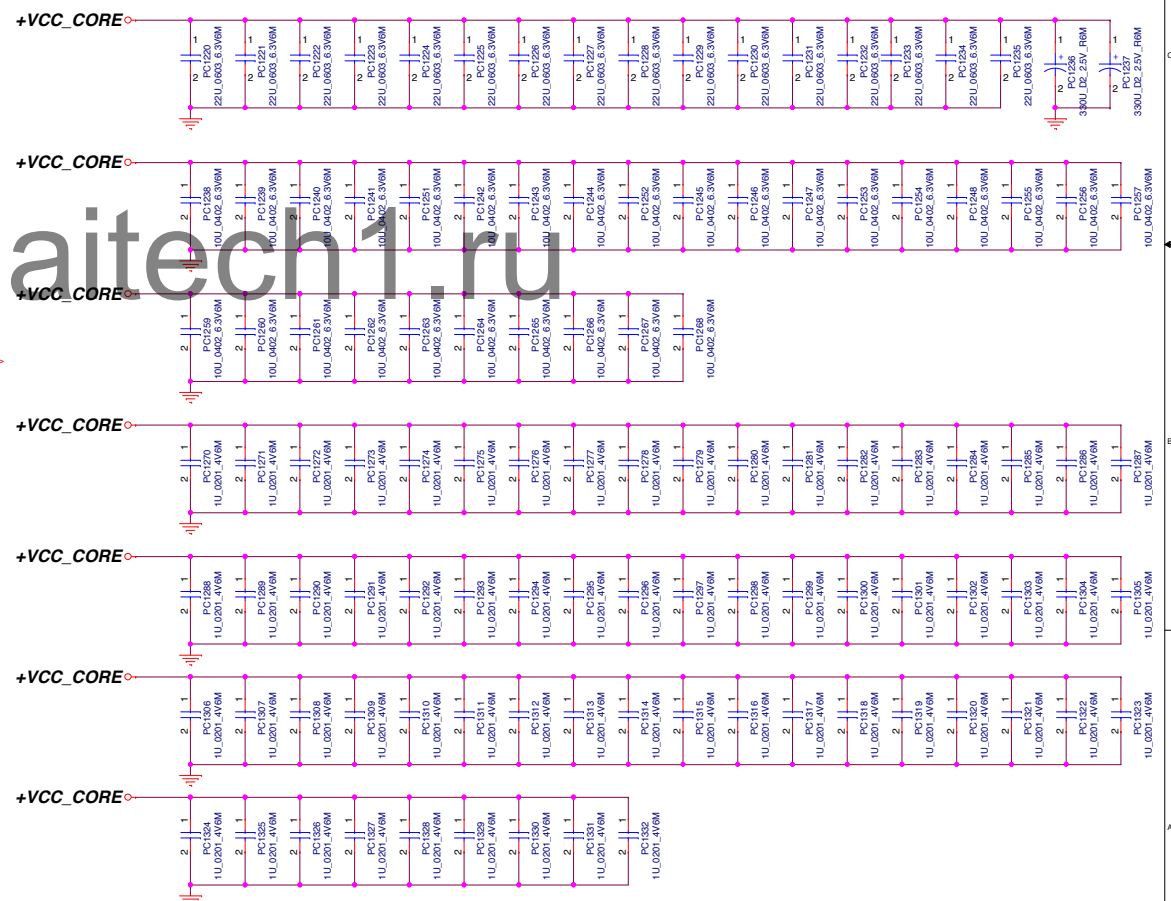
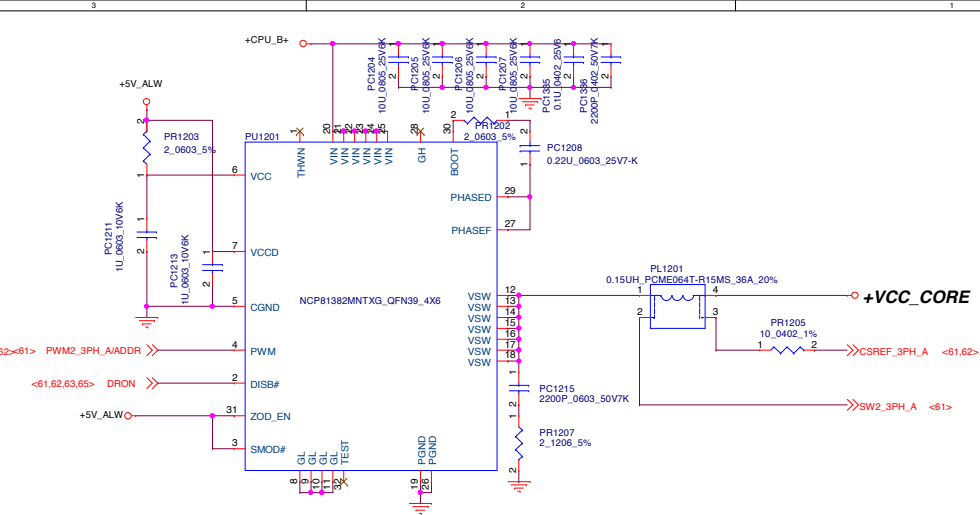
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Title			
+1.8V_ALW			
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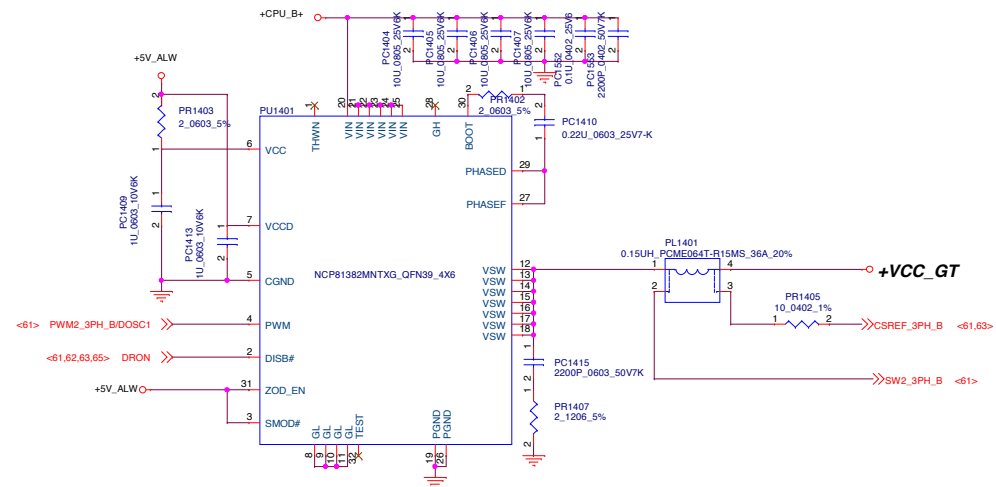
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	Title
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	Date

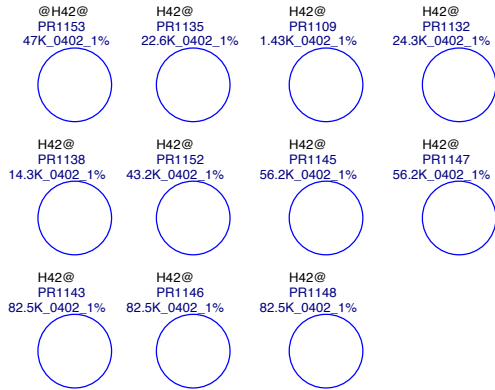
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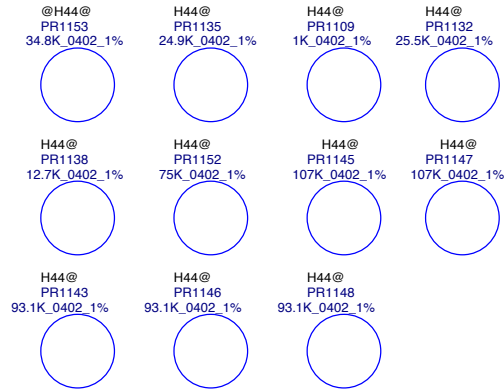
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	Title		
	+VCC_GT		
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C541_H42 component



C541_H44e component



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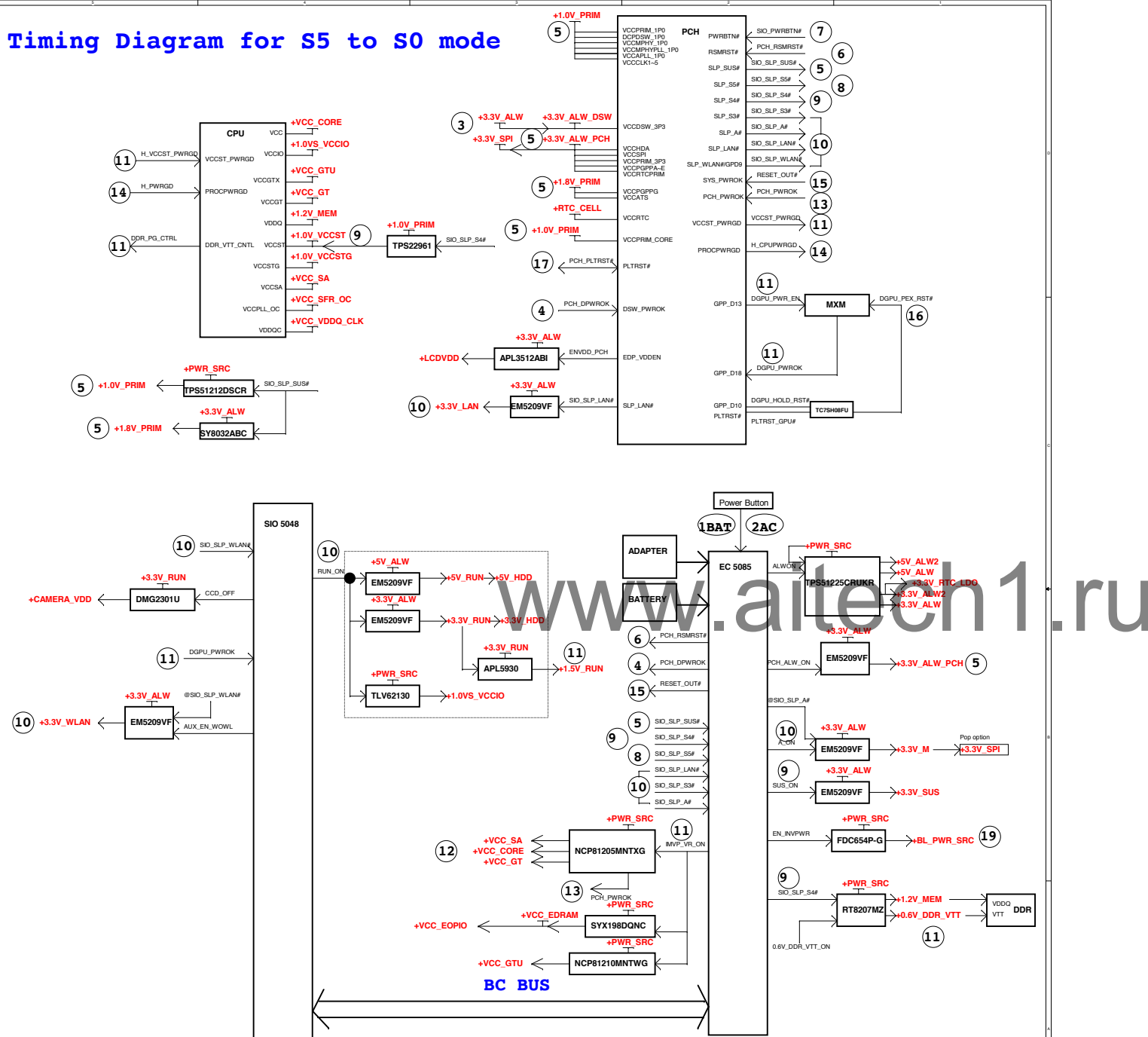
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PWR_table			
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Timing Diagram for S5 to S0 mode



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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	22, 37, 49	HW	12/6/2014	compal	reserve SPI and TPM PWR rail optional +3.3V_ALW_PCH or +3.3V_M.	Add RH343,RH344,RZ75,depop UZ28,C547,C513 for SPI and TPM PWR rail change to +3.3V_ALW_PCH,add @RH348 to +3.3V_M power rail option for +3.3V 1.8V SPI.	X01(0.2)
2	37, 46	HW	12/6/2014	compal	GPIO MAP:Gen7_GPIO1211	U51.B62 change netname from POA_EN to EC_FPM_EN and U51.A9 change netname from SUS_ON to CV2_ON for follow GPIO MAP	X01(0.2)
3	41	HW	12/6/2014	compal	correct U6 PWR rail to map U6 input level.	U6.5 PWR change from +3.3V_HDD to +1.0V_RUN for U6 input signal is 1.4V level.	X01(0.2)
4	45	HW	12/6/2014	compal	Avoid backdrive to +3.3V_RUN.	R3740.2(UPD_SMBUS_ALERT#) PWR rail change from +3.3V_RUN to +3.3V_ALW.	X01(0.2)
5	48	HW	12/6/2014	compal	TP I2C interface reserve 0ohm	add R3752,R3758	X01(0.2)
6	28, 35	HW	12/9/2014	compal	symbol link CIS normal CPN	update U8 symbol for SA00007ZW00,update U31 symbol for SA000081G0L	X01(0.2)
7	24	HW	12/9/2014	AMD	aviod incorrect behavior when system w/AMD MXM cards	Reserve a pull up 10k(RH345) to +3.3V_ALW_PCH close to PCH side on GPU_EVENT#	X01(0.2)
8	24	HW	12/10/2014	compal	FAN control SMBUS connect error	AAC_SMBCLK change to connect U8.20,AAC_SMBDAT change to connect U8.21 change U8.43 connect R371 then connect LED to GND	X01(0.2)
9	25, 30	HW	12/10/2014	compal	add "+" on PWR trace netname and others no "+"	add netname +DCPRTC on CH68.1,change netname +3.3V_CAM_EN# to 3.3V_CAM_EN#	X01(0.2)
10	38	HW	12/10/2014	compal	symbol CPN and Value not match.	change C1176,C1402 PN to SGA00002B00,and depop C1402	X01(0.2)
11	41	HW	12/11/2014	compal	double PU	remove @R3754	X01(0.2)
12	30	HW	12/11/2014	compal	align BC change Q24 main source	change Q24 to SB00000QP00	X01(0.2)
13	23	HW	12/15/2014	RF	RF request	change CH268 from 0.01uF to 22pF	X01(0.2)
14	45, 46	HW	12/17/2014	compal	Gen7 GPIO1211	remove R851,R852,R853,R854,change netname CPU_ID to GPIOLO,U51.A40 to MSDATA,U51.B43 to MSCLK,U51.B46 to PCH_PCIE_WAKE#,U46.A64 to ME_FW_EC,U46.A8 to USB_PWR_SHR_LFT_EN#	X01(0.2)
15	19, 42, 41	HW	12/19/2014	compal	SATA express HDD function issue-PCIE13-16 lane reverse	SATA express interface change to PCIE14(match HDD port1),PCIE13(match HDD port0),UH1.AG39 change to HDD_DET#,UH1.AD35 to SATA_EXP_IFDET.	X01(0.2)
16	46	HW	12/23/2014	compal	reserve for next-gen EC that use the Intel chipset UART TXD for the SBIOS Serouts	add R862,R863,change netname GPP_C9 to SBIOS_TX	X01(0.2)
17	46	HW	12/29/2014	compal	SB339045100 EOL	change Q28 to SB000008P00	X01(0.2)
18	22	HW	12/30/2014	compal	solve TPM PLTRST leakage	add RH346 and depop RH187,RH196, change U638.5 to 3.3V_ALW_PCH	X01(0.2)
19	6, 39, 35, 47, 22, 7, 36	HW	12/30/2014	compal	same Value a CPN on Board	PEG 0.22UF AC CAP(CC1-CC64) and SSD 0.22UF AC CAP(CN83,CN85-CN88,CN91,CN92,CN95,CN97)change from SE00000R700 to SE095224K00 U15,U58,U638,UC4 change from SA007080120 to SA007080180 Q327 change from SB00000ST00 to SB00000U000 T156 change from SP050006P00 to SP050006Y00	X01(0.2)
20	21	HW	12/30/2014	compal	DG1.0 RTC Crystal MAX ESR is 50Kohm	YH1 change to SJ10000LV00	X01(0.2)
21	42	HW	12/30/2014	compal	HDD SATA/PCIE repeater change to GEN3 chip	UN8,UN9 change from PS8555 to PS8558(SA00008DT00),CN75,CN71 change to 0.01uF,CN70,CN63,CN69,CN76,CN64,CN72,CN79,CN65,CN74,CN80,CN66,CN81 change to 0.22uF,remove CN77,CN68,CN82,CN78,add RH99-RH111,RH114-RH130	X01(0.2)
22	23	HW	12/31/2014	compal	MOW Rev1.0-To enable Direct Connect Interface (DCI),a 150K pull up resistor will need to be added to PCHHOT# pin.	RH329 change to 150kohm(SD028150380) and pop it,reserve RH347 pull up to +3.3V_RUN,add RH353,@QH5	X01(0.2)
23	37	HW	01/05/2015	compal	System will shut down as soon as system power on with FPM and RFID/NFC testing result is failed	add DZ3,RZ76,RZ72,RZ73.change JUSH1.9 from +5V_ALW2 to +5V_ALW, JUSH1.10 from +3.3V_ALW2 to +5V_ALW2,JUSH1.25 from GND to +3.3V_ALW2, JUSH1.26 from GND to +PWR_SRC.	X01(0.2)
24	39	HW	01/06/2015	compal	no business with vender-KEMET	change C619 from SGA00000N00 to SGA00002B00	X01(0.2)

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25	15, 17	HW	01/06/2015	compal	CONN LIST1124	change JDIMM2 to ADDR0106-P005A, JDIMM4 to ADDR0107-P005A	X01(0.2)
26	46	HW	01/06/2015	compal	Board ID	change R875 to 130Kohm(SD028130380)	X01(0.2)
27	28	HW	01/08/2015	compal	Follow FAN CONTROL DEBUG tool connector PIN define	remove SWV_DBG from JDEG3.4, change JDEG1 PIN define.	X01(0.2)
28	28	HW	01/08/2015	compal	USH SMBUS PULL UP when wo/ USH/B	remove R3738,R3739,Q366 BS AAC@(let them always pop w/USH or wo/USH)	X01(0.2)
29	21	HW	01/08/2015	compal	Crystal EA	change CH13,CH14 from 22pF to 15pF.	X01(0.2)
30	40, 30	HW	01/08/2015	compal	for Battery life measure	add PJP25,PJP26	X01(0.2)
31	18, 20, 30	HW	01/08/2015	compal	cost saving	change U17,UC3 from SA00003Y000 to SA000046R00,U33 from SA00003AR00 to SA00006Y800 and add @R42,change Q21 from SB000009K10 to SB000010C00	X01(0.2)
32	46	HW	01/08/2015	compal	EC5085 change CPN	change U51 to SA00006YH60	X01(0.2)
33	22	HW	01/09/2015	compal	ADD PWR net on pin16 of JSPi1	netname is +3.3V_SPI_R on JSPi1.16	X01(0.2)
34	22	HW	01/09/2015	compal	PLTRST group change balance before AND GATE and after	add RH349,@RH350,change RH210.1 to PCH_PLTRST#,RH337.1 to PCH_PLTRST#_AND,RH195.1 to PCH_PLTRST#	X01(0.2)
35	24	BIOS	01/13/2015	compal	AMI BIOS Bidirection debug	remove dummy net PCH NFC RST,add RH351,RH352 PU to +3.3V_ALW_PCH and add @RH354,@RH355 PU to +3.3V_RUN on UH1.AR39,UH1.AR45,add JUART1	X01(0.2)
36	14	HW	01/14/2015	compal	MOW rev1.0 ww02- recommended not to install any capacitor on DDR Reset signal (DRAMRST)	depop CD16	X01(0.2)
37	28	HW	01/19/2015	compal	resevrve AAC SMBUS control from PCH	add R38,R39,@R40,@R41,and R40.2 connect to UH1.AT42, R41.2 connect to UH1.AR38	X01(0.2)
38	47	ME	01/19/2015	compal	Screw hole	remove H26,H28,add H30,change H1,H2,H3,H4 from H_4P2 to H_3P8	X01(0.2)
39	10, 11	HW	01/20/2015	intel	VENDER suggestion	remove RC218,@RC219,@RC311	X01(0.2)
40	28	HW	01/20/2015	COMPAL	ARD1.3	connect FAN1 TACH_FB_AAC to U8.24,FAN2 TACH_FB_AAC to U8.25,FAN1 TACH_EC_AAC to U8.26,FAN2 TACH_EC_AAC to U8.27	X01(0.2)
41	47	HW	01/20/2015	COMPAL	LED limit current R value	change R956,R955 to 1kohm,R130,R131,R943 to 560ohm	X01(0.2)
42	31, 32	HW	01/20/2015	COMPAL	DOCK DP1,DP2 EA	pop R117,R119,R121(AEQ disable,PEQ=8.5dB),RV29,RV35(PEQ=8.5dB)	X01(0.2)
43	37	HW	01/21/2015	COMPAL	TPM improve S3 support and back drive issue	Add RZ78,@RZ79,@RZ77,@RZ80,QZ2,RZ82,change U637.1 to +3.3V_ALW_PCH,U637.8 to +U637_TPM,U637.12 to NC	X01(0.2)
44	30	HW	01/22/2015	COMPAL	TOUCH_SCREEN_PD# PU PWR rail align with PC	change R426.1 to +3.3V_RUN	X01(0.2)
45	7	HW	01/26/2015	COMPAL	Solving for when system force shut down,it can't power on with power botten between 1 minute.	add @R43,@RC327,UC5,UC6	X01(0.2)
46	7	HW	01/26/2015	INTEL	DCI debug-when no XDP function,we can debug CPU and PCH from USB interface	change RC307,RC308,RC309,RC143 Bom Structure from XDP@ to always pop.	X01(0.2)
47	35	HW	03/16/2015	COMPAL	LAN EA	change L63-L70 to 0ohm(R63-R70)	X02(0.3)
48	20	HW	03/16/2015	INTEL	546717_SKL_PCH_H_EDS_R1_2(add a 1K PD for USB2 VBUSSENSE, if the signal is not used.Else it impacts Intel DCI test with warm boot),546765_WM10_MOW_USB2_ID connected directly to GND,if platform no support dual role	add RH356,RH357 pull down to GND.	X02(0.3)
49	43	HW	03/16/2015	COMPAL	DOCK E-SATA signal reverse.	SWAP SATA_PTX_C_DRX_P1 to JDOCK1.60(C699.1),SATA_PTX_C_DRX_N1 to JDOCK1.62(C700.1)	X02(0.3)
50	28	HW	03/16/2015	COMPAL	FAN module keep EVT pin define,FAN connector pin define of MB need change to meet it from H type to V type.	change JFAN1,JFAN2 pin define to PIN1=+5V_RUN,PIN2=FB,PIN3=PWM,PIN4=GND	X02(0.3)
51	37	HW	03/16/2015	VENDER	reserve @RZ83 for modern standby,RZ84 for TPM detect issue.	add RZ83 connect to SIO_SLP_S0#,RZ84 between PCH_SPI_CS#2_R and QZ2.2, pop RZ79,depop RZ78.	X02(0.3)

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52	30	HW	03/16/2015	compal	reserve IR camera layout.	change JTS1 from 6pin to 10pin,add +BL_PWR_SRC on JTS1.9, JTS1.10 and add GND on JTS1.7,JTS1.8	X02(0.3)
53	23	RF	03/16/2015	compal	RF EA	pop CH42,CH49,CH50,CH51	X02(0.3)
54	30	HW	03/16/2015	compal	for AAC function	pop R361,R362	X02(0.3)
55	46	HW	03/17/2015	compal	material lack	change R374 from SD014430280 to SD034430280	X02(0.3)
56	18	HW	03/18/2015	compal	solve never detect Hot plug event input at Optimus GPU off	add R71,C1470,D95,R72change U14.1,U25.1,U27.1 from DGPU_PWROK to DGPU_PEX_RST#_D,remove @C95,@C96	X02(0.3)
57	24	HW	03/19/2015	compal	reserve DIMM TYPE selection	add RH358	X02(0.3)
58	47	HW	03/19/2015	compal	LED luminance adjust	change R943 from 560ohm to 1Kohm,R956 from 1Kohm to 430ohm	X02(0.3)
59	47	HW	03/24/2015	compal	screw hole	change H15 from NPTH to PTH	X02(0.3)
60	7	HW	03/24/2015	compal	XDP working	depop RC314,RC315,add RC328	X02(0.3)
61	44	HW	03/24/2015	compal	Keep VBUS PWR stable	change JIO2.17 from +PWR_SRC to +VBUS_DC_SS	X02(0.3)
62	7,23	HW	03/24/2015	compal	backdrive and DG1.0	change RH312.1,RH314.1,RH315.1 from +1.0V_VCCSTG to +1.0V_VCCST	X02(0.3)
63	21,46	HW	03/24/2015	compal	Crystal EA	change C741,C743 from 22pF to 33pF,CH4 from 18pF to 12pF,CH5 from 18pF to 15pF	X02(0.3)
64	24,30	HW	03/25/2015	compal	IR camera detect pin for verb table	add GPP A23 to IR_CAM_DET# and connect to JEDP1 pin26,add R366 pull up to +3.3V_RUN	X02(0.3)
65	46	HW	03/30/2015	compal	board ID	change R875 from 130Kohm to 33Kohm	X02(0.3)
66	38	RF	04/21/2015	compal	reserve SIM detection design	add RZ113 between SIM pin1(JSIM1) to WWAN pin58(JNGFF2)	X03(0.4)
67	48	HW	04/21/2015	compal	TP module add damping R,PU and new touchpad support PS2(in DOS),I2C bus(in OS)	add R370,R400(PS2),depop R3752,R3758,add RZ116,RZ117 pull up to +3.3V_TP	X03(0.4)
68	45	HW	04/24/2015	compal	BITS211484: Left IO/B USB port 1 can't charge smart mobile device under S3/S4/S5	add RE72,RE73,RE74,RE75,RE76 pull up to +3.3V_ALW.	X03(0.4)
69	28	HW	04/27/2015	DELL	AAC update BOM for mic	change C1420 and C365 from 0.1uf to 2.2uF.	X03(0.4)
70	22	HW	04/27/2015	boardcom	USH reset by BCM58102	depop RH359	X03(0.4)
71	24,30	HW	05/18/2015	DELL	back to without IR support	Change TS1 from 10pin(ACES 50228-01071-001)to 6pin(ACES 50228-0067N-001),remove IR_CAM_DET# netname and R366.	X03(0.4)
72	22,30	HW	05/18/2015	DELL	Add Touch screen detect signal	Add TOUCH_SCREEN_DET# on UH1.BD24 and JTS1.5, Add R382 PU to +3.3V_RUN,and remove RH336.	X03(0.4)
73	18	HW	05/18/2015	NVIDIA	add test pad on DVI_HPD of MXM	Add T217 on DVI_HPD	X03(0.4)
74	46	HW	05/18/2015	compal	common EC code	change U51 from SA00006YH60 to SA00006YH30.	X03(0.4)
75	47	HW	05/18/2015	compal	HDD active LED behavior for PCIe M.2 SSD module	add D97,D98,D99,@R389,and add R383 PU to +3.3V_RUN,R384 PU to +3.3V_WWAN,R385 PU to +3.3V_SSD1	X03(0.4)
76	48	HW	05/21/2015	compal	BOM change for Touchpad function	pop CZ30,CZ31 and change them to 100pF	X03(0.4)
77	47	ME	05/21/2015	compal	Screw hole change	remove H11,H24,add H31	X03(0.4)
78	44,45	PWR	05/21/2015	compal	TBT PD power support	change JIO2.36 from GND to DCIN_ACOK#,and add PROCHOT_GATE on U46.A61	X03(0.4)
79	45	BIOS	05/22/2015	compal	EC detect for AR/B or non AR/B	change JIO2.34 from GND to PD_ACE_DET#_R,and add R388 between U46.A60 and PD_ACE_DET#_R.add RE77 PU to +3.3V_ALW	X03(0.4)
80	46	HW	05/22/2015	compal	board ID	change R875 from 33Kohm to 4.3Kohm	X03(0.4)
81	41,47	HW	05/22/2015	compal	BITS224631 [DVT1.1 M15/17]HDD LED indicator not light if use NVMe SSD	add U639,R386,D100,and add R387 PU to +3.3V_RUN	X03(0.4)

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82	26	HW	06/03/2015	compal	reserve 0.1uF for 5.76G noise	add @CH269	X04(0.5)
83	46	HW	06/03/2015	compal	Board ID	change R875 from 4.3kohm to 2kohm	X04(0.5)
84	44	HW	06/03/2015	compal	GPIO pin can direct PU/PD no need serise R to limilt current	change R388 from 10kohm to 0ohm	X04(0.5)
85	38	HW	06/03/2015	compal	SSD support gen3	change CZ1,CZ2,CZ91,CZ92 from 0.1uF to 0.22uF,remove CZ23,CZ24,add RZ118,RZ119	X04(0.5)
86	38	HW	06/04/2015	compal	WLAN module still need support LAN disable	pop D31	X04(0.5)
87	22	HW	06/08/2015	compal	QS CPU no need PD on SPI0_IO3 for boot	depop RH334	X04(0.5)
88	18	HW	06/11/2015	compal	MXM3.1 SPEC	remove @R6,@R1979,change JMXM1 pin268,pin270 to +3.3V_MXM	X04(0.5)
89	19,45	HW	06/11/2015	compal	reserve GPIO pin for tell EC don't read GFX Temp.in GC6	connect RH342.1 to U46.A48,remove R3749	X04(0.5)
90	45	HW	06/11/2015	compal	PROCHOT_GATE initial status	add @R415 PU to +3.3V_ALW,R416 PD to GND	X04(0.5)
91	49	HW	06/15/2015	compal	Dirty shutdown	add R417(PCH_ALW_ON)and @R418(SIO_SLP_SUS#_R)option select turn on +3.3V_ALW_PCH	X04(0.5)
92	46	HW	07/05/2015	compal	power on/off sequence tCPU05/tPLT18/tCPU03 and global reset issue	add U9,@C787 for tCPU05 and tPLT18,add RC329,CC273 for tCPU03,add @Q370,R435 for global reset	X05(0.6)
93	37	HW	07/05/2015	compal	TPM DS3 support	change U637.1 from +3.3V_ALW_PCH to +3.3V_ALW	X05(0.6)
94	46	HW	07/05/2015	compal	Board ID	change R875 from 2kohm to 1kohm	X05(0.6)
95	42	HW	07/29/2015	compal	SATA IEMT CTLE(change RX EQ from level 1 to 2)	pop RN130	1.0(A00)
96	41	HW	07/29/2015	compal	SATA PWR supply for over loading	pop C404,change C403 for 0.1uF to 22uF,and pop it.	1.0(A00)
97	11	HW	07/31/2015	compal	VCCPLL_OC power gate requirement for Deep Sleep support	depop RC302,add UZ30,@RC330,@CZ95,@CZ96,CZ97,UC7,@CZ98	1.0(A00)
98	46	HW	08/03/2015	compal	Board ID	change R875 from 1kohm to 62kohm	1.0(A00)
99	7,23	HW	08/07/2015	compal	backdrive and CPU EDS0.95	change RC135.1,RH312.1,RH314.1,RH315.1 from +1.0V_VCCST to +1.0V_VCCSTG	1.0(A00)
100	22,35,46	HW	08/07/2015	compal	MP component CPN	change UH1 to SA00009602L,U31 to SA000081G1L,U51 to SA00006YH90	1.0(A00)
101	7,23,28,30,44,49	HW	08/13/2015	compal	MP BOM change	depop R3739,R3738,R40,R41,U8,C31-C36,R23-R30,C141,C143,C365,C1420,R373,R375,R414,R410,R413,R411,R361,R362(drop AAC),SW1,SW2,R3728,UZ28,C513,C547,pop RC301	1.0(A00)
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1	P57	POWER	1/6	COMPAL	BQ24780 IFAULT LOW latch off	1. PC702 chagne to 0.1uF 2. PC704 change to 0.01uF	PR02
2	P51	POWER	1/6	COMPAL	PU101 change to TPS51285B	1. PU101 change to TPS51285B 2. PC100/PC118 chagne to 4.7uF 3. add PR114 4. PR105 change to 29.4k ohm 5. PR106 change to 31.6k ohm	PR02
3	P64	POWER	1/19	COMPAL	VCC_GTU sense	Add PR1620/PR1621 100ohm	PR02
4	P61	POWER	1/28	COMPAL	VCORE parameter adjust for vendor request	1. PR1109 change to 1.43k ohm 2. PR1137/PR1133 change to 3.65k ohm 3. PC1121/PC1124 change to 100pF 4. PR1132 change to 25.5k ohm 5. PC1123/PC1125 change to 0.1uF 6. PC1104 change to 2200pF 7. PR1112 change to 30k ohm 8. PC1107 change to 6800pF 9. PR1135 change to 24.9k ohm 10. PR1152 change to 75k ohm	PR02
5	P52	POWER	3/18	COMPAL	change unmount for HW request(power sequence)	PC215 change to numount	PR03
6	P53	POWER	3/18	COMPAL	Add RC for HW request(Power sequence)	Add PR317/PC312	PR03
7	P57	POWER	3/18	COMPAL	change to connect RENG for BATTERY reverse input protection	Add PD703 in IC RENG pin	PR03
8	P64	POWER	3/18	COMPAL	change VCC_GTU parameter for Vendor request	PR1604 change to 6.19k ohm add PC1690 to 4700p F	PR03
9	P57 P60	POWER	3/24	COMPAL	Add circuit to prevent +SDC_IN oscillation	Add PD704/PR766~PR770/PQ708 Add PD1101/1033~PR1037/PQ1005	PR03

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10	P61	POWER	3/26	COMPAL	Add PR1170 for CPU H LINE-42	Add PR1170	PR03
11	P57	POWER	4/29	COMPAL	change CHARGER parameter for Vendor request	PR744 change to 45.3k ohm	PR03
12	P57	POWER	4/30	COMPAL	Add circuit to detect type C current	Add PQ1073(SB000000DH00) /PR771(SD028000080) ,PR772(SD034100380) ,PR773(SD028000080)	PR04
13	P61	POWER	4/30	COMPAL	change VCORE parameter for IPCC solution	PR1153 change to 34.8k ohm(H44e) 、47kohm(H42)	PR04
14	P60	POWER	5/8	COMPAL	Add circuit for avoiding type C current to flow to battery	Add PD1102/ PD1103(SCS0340L010)/ PR1026 100 ohm(SD014100080)	PR04
15	P57	POWER	5/14	COMPAL	Change the charger ILIM circuit for current sense	PR758 from 18K to 20K、PR760 from 3.16K to 5.36K and PR764 from 20K to 2.74K	PR04
16	P57	POWER	5/19	COMPAL	Add circuit for the PD	Add PC151(SE102104K00)/ PQ1074(SB000000DH00)/ PU105(SA007080120)	PR04
17	P50	POWER	6/8	COMPAL	Add diodes for ESD team request	Add PD4/PD6(SCA00000T00)	PR05
18	P50	POWER	6/15	COMPAL	Change PU1 for ESD issue	Change PU1 from SA00003DN00 to SA00001WK00/ depop PD4/PD6	PR05
19	P61	POWER	6/23	COMPAL	change VCORE parameter for IPCC solution	PR1153 change to 30.9Kohm(SD034309280)	PR05
20	P52 P53	POWER	7/6	COMPAL	For tCPU05 (VDDQ 1.2V to VCCIO 1.0V) add one AGATE 7408 and control by SIO_SLP_S3# and 1.2V_SUS_PWRGD(for HW)	Depop PC312/PR303 Remove PR317 Change EC netname(to HW) from SIO_SLP_S3# to RUN_ON_AND Pop PR209 Add offpagethe for 1.2V_SUS_PWRGD	PR06

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